ADM6999G - 8 port 10/100 Mb/s + Gigabit Single Chip Ethernet Switch Controller

Data Sheet

Revision 1.3

May 2003

Revision History

Revision Date	Revision	Description
Aug/2002	0.1	First Infineon ADMtek Co Ltd version
Sep/2002	1.0	Remove Preliminary word
Dec/2002	1.1	Modify error word. Add GMII timing.
Apr/2003	1.2	Modify GMII receive setup time and hold time. GRXER change to GND or NC. Modify MII RXCLK & TXCLK timing requirement.
May/2003	1.3	Modify RTX to 1K 1% at A2 version chip.
Apr/2004	1.4	Updated logo to Infineon-ADMtek Co Ltd

Notice:

This document contains preliminary information on new products under development.

The specifications are subject to change without any further notice.

Please contact Infineon ADMtek Co Ltd sales to ensure the updated specifications before finalizing your own design.

1. Introduction

1.1 General Descriptions

The ADM6999G is a high performance, low cost, highly integration (Controller, PHY and Memory) eight-port 10/100 Mbps TX/FX plus one 10/100/1000 GMII port Ethernet switch controller with all ports supporting 10/100 Mbps Full/Half duplex and Gigabit port support Full Duplex switch function. The ADM6999G is intended for applications to stand alone bridge for low cost SOHO market such as 8+1G.

ADM6999G provides most advance function such as: **802.1p(Q.O.S.), 802.1q(VLAN), Port MAC address Locking, Management, Port Status, TP Auto-MDIX, 25M Crystal & Extra ninth port (GMII)** function to meet customer request on Switch demand.

The built-in 768K SRAM used for packet buffer and address learning table is divided into 512 bytes/block to achieve the optimized memory utilization through complicated link list on packets with various lengths.

ADM6999G also supports priority features by Port-Base, VLAN and IP TOS field checking. User can be easy to set as different priority mode in individual port, through a small low-cost micro controller to initialize or on-the-fly to configure. Each output port supports two queues in the way of fixed N: 1 fairness queuing to fit the bandwidth demand on various types of packet such as Voice, Video and data. 802.1Q, Tag/Untag, and up to 32 groups of VLAN also is supported. ADM6999G learns user define 4 or 5 bits of VLAN ID.

An intelligent address recognition algorithm makes ADM6999G to recognize up to 2048 different MAC addresses and enables filtering and forwarding at full wire speed.

Port MAC address Locking function is also supported by ADM6999G to use on Building Internet access to prevent multiple users share one port traffic.

1.2 Features

- ✔ Supports eight 10M/100M auto-detect Half/Full duplex switch ports with **TX/FX** interfaces and one GMII/MII port.
- ✔ Built-in 12Kx64 SRAM.
- ✔ Supports 2048 MAC addresses table.
- ✔ Supports two queue for Qos
- ✔ Supports priority features by Port-Based, 802.1p VLAN & IP TOS of packets.
- ✔ Supports Store & Forward architecture and performs forwarding and filtering at non-blocking full wire speed.

- ✔ Supports buffer allocation with 512 bytes per block
- ✔ Supports Aging function Enable/Disable.
- ✔ Supports serial Single/Dual color mode with Power On auto diagnostic.
- ✔ Supports 802.3x Flow Control pause packet for Full Duplex in case buffer is full.
- ✔ Supports Back Pressure function for Half Duplex operation in case buffer is full.
- ✔ Supports packet length up to 1522 bytes.
- ✔ Broadcast Storming Filter function.
- ✔ Supports 802.1Q VLAN. Up to 16/32 VLAN groups is implemented by user define four/five bits of VLAN ID.
- ✔ Support MAC-clone feature
- ✔ Supports TP interface **Auto MDIX** function for auto TX/RX swap by strapping-pin.
- ✔ Easy Management 32bits smart counter for per port RX/TX byte/packet count, error count and collision count.
- ✔ Support PHY status output for management system.
- ✔ 25M Crystal only for the whole system. Output 25M/125M for different interface.
- ✔ 128 QFP package with 0.18um technology. 1.8V/3.3V power supply.

1.3 Applications

ADM6999G in 128-pin PQFP:

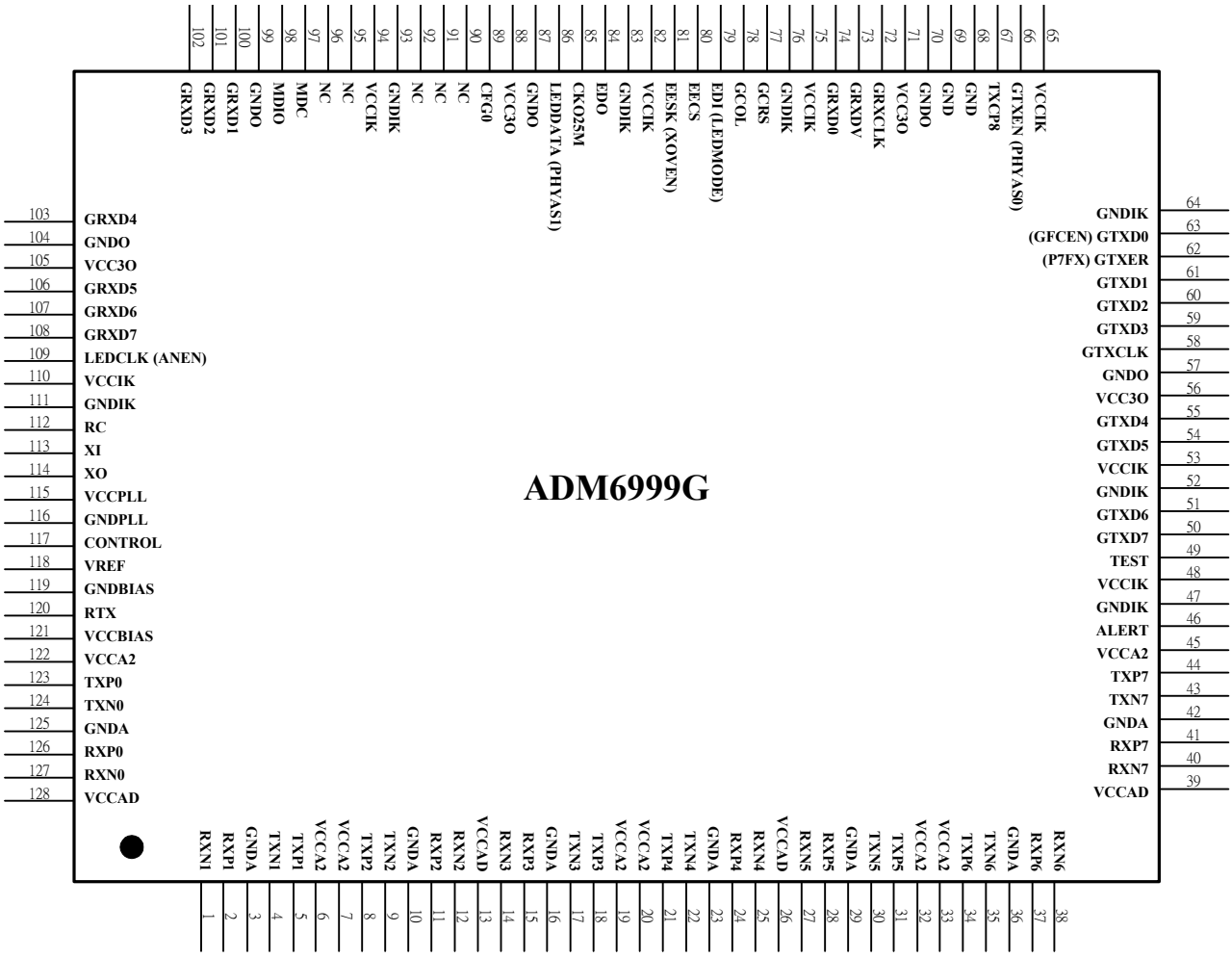
Standalone SOHO 8+1 Gigabit Switch as start-kit

Gigabit up link module, etc…

2. Pin Out

2.1 Pin Diagram

8 TP/FX PORT + 1 GMII PORT 128 Pin Diagram



2.2 Pin Description

Pin Type I: Input, O: Output, I/O: Bi-directional, OD: Open drain, SCHE: Schmitt Trigger

PD : internal pull-down, PU : internal pull-up

Note: Do not swap TP port +-. It may cause link fail when link partner does not support Auto Polarity function.

Pin #	Pin Name	Pin Type	Pin Description
			Twisted Pair Interface
126, 2, 11 15, 24, 28 37, 41	RXP[0:7]	I/O, Analog	**Twisted Pair Receive Input Positive.**
127, 1, 12 14, 25, 27 38, 40	RXN[0:7]	I/O, Analog	**Twisted Pair Receive Input Negative.**
123, 5, 8 18, 21, 31 34, 44	TXP[0:7]	I/O, Analog	**Twisted Pair Transmit Output Positive.**
124, 4, 9 17, 22, 30 35, 43	TXN[0:7]	I/O, Analog	**Twisted Pair Transmit Output Negative.**
			9th Port(GMII) Interface
63	GTXD[0] **Setting** GFCEN	I/O, 8mA PU	**Giga Port transmit data 0** Acts as GMII transmit data TXD0 synchronous to the rising edge of TXCLK. **Setting** GFCEN: Global Flow Control Enable. At power-on-reset, latched as Full Duplex Flow control setting "1" to enable flow-control (default), "0" to disable flow-control.
50,51,54, 55,59,60, 61	GTXD[7:1]	O, 8mA	**Giga Port Transmit Data bit 7~1** Synchronous to the rising edge of GTXCLK.
62	GTXER **Setting** P7FX	I/O 8mA PD	**Giga Port Transmit Error** **Setting** P7FX: Setting Port7 FX/TX mode select. Internal pull down. 1: Port7 as FX port. 0: Port7 as TX port.

66	GTXEN **Setting** PHYAS0	I/O 8mA PD	**Giga Port Transmit Enable.** **Setting** PHYAS0: Chip physical address0 for multiple chip application on EEPROM access. Internal pull down. Power on reset value PHYAS0 combines with PHYAS1(LEDDATA). PHYAD Gigabit PHY Address 00 08h Master Master: ADM6999G will read 93C46 EEPROM first Bank.(00h~27h). If there is no EEPROM then user must use 93C66 timing to write chip's register. If user put 93C46 with correct Signature then user writes chip register by 93C46 timing. If user put 93C66 then data put in Bank0. User can write chip register by 93C66 timing. User must assert one SK cycle when CS at idle stage when write chip internal register.
108,107,106, 103,102,101, 100,74	GRXD[7:0]	I PD	**Giga Port receive data 7~0** Synchronous to the rising edge of RXCLK.
73	GRXDV	I PD	**Giga Port receive data valid.** Internal pull down.
68	GND	I PD	**GND or NC at normal application.**
78	GCOL	I PD	**MII Port Collision input** Internal pull down.
77	GCRS	I PD	**Giga Port Carrier Sense** Internal pull down.
58	GTXCLK	O 16mA	**Gigabit Port 125MHz clock Output**
72	GRXCLK	I	**Giga Port Receive Clock Input**
67	TXCP8	I	**MII Port Transmit clock Input**
LED Interface			
86	LEDDATA **Setting** PHYAS1		**Serial LED Data** **Setting** PHYAS1: Chip physical address1 for multiple chip application on EEPROM access. Internal pull down. See pin 66.
109	LEDCLK **Setting** ANEN		**Serial LED Clock** **Setting** ANEN: On power-on-reset, latched as Auto Negotiation capability for all ports. "1" to enable Auto Negotiation (defaulted by pulled up internally), "0" to disable Auto Negotiation.
EEPROM/Management Interface			
84	EEDO	I, TTL PU	**EEPROM Data Output.** Serial data input from EEPROM. This pin is internally pull-up.

80	EECS	O, 4mA PD	**EEPROM Chip Select.** This pin is active high chip enable for EEPROM. When RC is low, it will be Tri-state. This pin is internally pull-down.
81	EECK **Setting** XOVEN	I/O, 4mA PD	**Serial Clock**. This pin is clock source for EEPROM. When RC is low, it will be tri-state. **Setting** XOVEN: This pin is internally pull-down. On power-on-reset, latched as P7~0 Auto MDIX enable or not. "1" to enable MDIX , "0" to disable MDIX (defaulted) **Suggest externally pull up to enable MDIX for all ports.**
79	EEDI **Setting** LEDMODE	O, 4mA PD	**EEPROM Serial Data Input.** This pin is output for serial data transfer. When RC is low, it will be tri-state. **Setting** LEDMODE: This pin is internal pull-down.. On power-on-reset, latched as Dual Color mode or not. 1: Dual Color LED. 0: Single Color LED.
98	MDIO	I/O, 8mA	**Management Data.** This pin is in-out to PHY. When RC is low, this pin will be tri-state.
97	MDC	O, 8mA	**Management Data Clock.** This pin output 1MHz clock to drive PHY and access corresponding speed and duplex data through MDIO.
		MISC	
85	CKO25M	O, 8mA	25M Clock Output For GMII port
117	Control	O	**FET Control Signal.** The pin is used to control FET for 3.3V to 1.8V regulator. Add 0.01uF capacitor to GND.
120	RTX	Analog	**TX Resistor.** Add 1.1K %1(A1), 1K %1(A2) resister to GND.
118	VREF	Analog	**Analog Reference Voltage.**
112	RC	I, SCHE	**RC Input for Power On reset.** Reset input pin.
113	XI	I, Analog	**25M Crystal Input.** 25M Crystal Input. Variation is limited to +/- 50ppm.
114	XO	O, Analog	**25M Crystal Output.** When connected to oscillator, this pin should left unconnected.
49	TEST	I, TTL	**TEST Value.** At normal application connect to GND.
		Chip configuration	
89	CFG0	I,TTL PU	Must Connected to GND.
46	ALERT	O	**Alert LED Display.** This pin will show the status of power-on-diagnostic and broadcast traffic.
		Power/Ground	
3, 10, 16, 23, 29, 36, 42, 125	GNDA	I	**Ground Used by AD Block.**
6, 7, 19,	VCCA2	I	**1.8V, Power Used by TX Line Driver.**

20, 32, 33, 45, 122			
13, 26, 39, 128	VCCAD	I	**3.3V, Power Used by AD Block.**
119	GNDBIAS	I	**Ground Used by Bias Block.**
121	VCCBIAS	I	**3.3V, Power Used by Bias Block.**
116	GNDPLL	I	**Ground used by PLL**
115	VCCPLL	I	**1.8V, Power used by PLL**
47, 52, 64, 76, 83, 93, 111	GNDIK	I	**Ground Used by Digital Core**
48, 53, 65, 75, 82, 94, 110	VCCIK	I	**1.8V, Power Used by Digital Core**
57, 70, 87, 99, 104	GNDO	I	**Ground Used by Digital Pad**
56, 71, 88, 105	VCC3O	I	**3.3V, Power Used by Digital Pad.**
69	GND	I, TTL	**Scan Enable.** This pin will be used as the scan enable input for testing. Connect to GND at normal application.
NC pins			
90,91,92, 95,96	NC		

3. Descriptions

3.1 Functional Descriptions

The ADM6999G integrates eight 100Base-X physical sub-layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, eight complete 10Base-T modules, 8 port 100/10 switch controller and one 10/100/1000 MAC and memory into a single chip for both 10Mbits/s, 100Mbits/s, 1000Mbits/s Ethernet switch operation. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either Full Duplex mode or Half-Duplex mode in 10Mbits/s and 100Mbits/s, Full duplex only at 1000Mbits/s operation. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The ADM6999G consists of three major blocks:

- 10/100M PHY Block
- Switch Controller Block
- Built-in 12Kx64 SSRAM

3.2 10/100M PHY Block

The 100Base-X section of the device implements he following functional blocks :

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair transceiver (PMD)

The 100Base-X and 10Base-T sections share the following functional blocks :

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

3.2.1 100Base-X Module

The ADM6999G implements 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 2. Bypass options for each of the major functional blocks within the 100Base-X PCS provides flexibility for various applications. 100Mbits/s PHY loop back is included for diagnostic purpose.

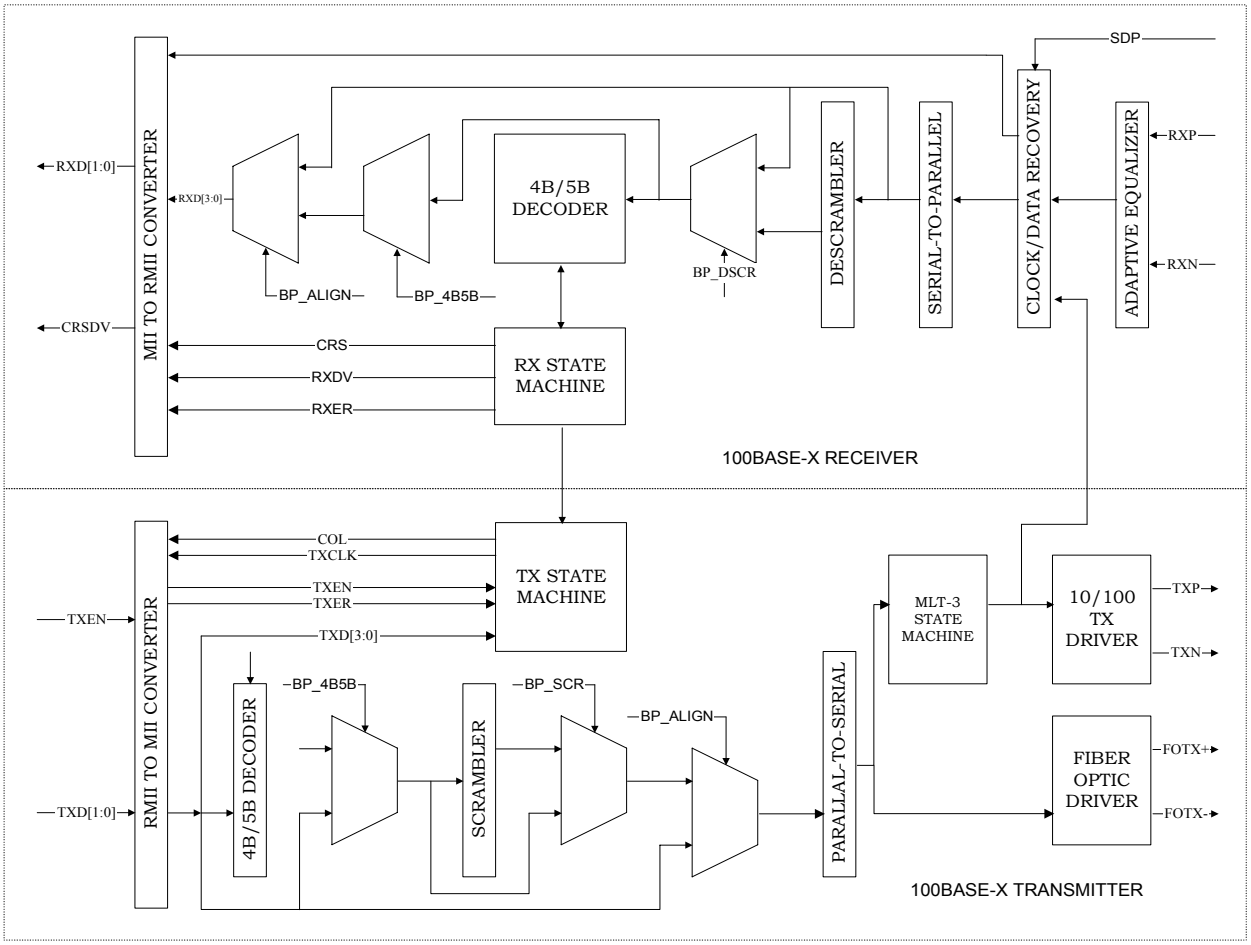
3.2.2 100Base-X Receiver

The 100Base-X receiver consists of functional blocks required to recover and condition the 125Mbits/s receive data stream. The ADM6999G implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125Mbits/s receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks :

- A/D Converter
- Adaptive Equalizer and timing recovery module

- NRZI/NRZ and serial/parallel decoder
- De-scrambler
- Symbol alignment block
- Symbol Decoder
- Collision Detect Block
- Carrier sense Block
- Stream decoder block



3.2.2.1 A/D Converter

High performance A/D converter with 125Mhz sampling rate converts signals received on RXP/RXN pins to 6 bits data streams; besides it possess auto-gain-control capability that will further improve receive performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

3.2.2.2 Adaptive Equalizer and timing Recovery Module

All digital design is especial immune from noise environments and achieves better correlation between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 120 meters.

3.2.2.3 NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

3.2.2.4 Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 us countdown. Upon detection of sufficient idle symbols within the 722 us period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize sufficient unscrambled idle symbols within 722 us period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

3.2.2.5 Symbol Alignment

The symbol alignment circuit in the ADM6999G determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

3.2.2.6 Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles as shown in Table 1. The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

3.2.2.7 Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

3.2.2.8 Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

3.2.2.9 100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The ADM6999G performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10Mbits/s link status to form the reportable link status bit in serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 us, and waits for an enable from the auto negotiation module. When receive, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

3.2.2.10 Carrier Sense

Carrier sense (CRS) for 100Mbits/s operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is de-asserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

3.2.2.11 Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM6999G will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles hat correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

3.2.2.12 Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

3.2.3 100Base-TX Transceiver

ADM6999G implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit

driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetic for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

3.2.3.1 Transmit Drivers

The ADM6999G 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.2.3.2 Twisted-Pair Receiver

For 100Base-TX operation, the incoming signal is detected by the on-chip twisted-pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits.

The ADM6999G uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

3.2.4 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop back, jabber, wave shaper, and link integrity functions, as defined in the standard. Figure 3 provides an overview for the 10Base-T module.

The ADM6999G 10Base-T module is comprised of the following functional blocks:

√ Manchester encoder and decoder
√ Collision detector
√ Link test function
√ Transmit driver and receiver
√ Serial and parallel interface
√ Jabber and SQE test functions
√ Polarity detection and correction

3.2.4.1 Operation Modes

The ADM6999G 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM6999G functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the ADM6999G can simultaneously transmit and receive data.

3.2.4.2 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

Decoding is accomplished by a differential input receiver circuit and a phase-locked loop that separate the

Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is de-asserted.

3.2.4.3 Transmit Driver and Receiver

The ADM6999G integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.2.4.4 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receive. The ADM6999G implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The signal at the start of the packet is checked by the analog squelch circuit and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.
Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 10 of register address 11h.

3.2.5 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbits/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbits/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.2.6 Jabber Function

The jabber function monitors the ADM6999G output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 256 ms (The un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 4 of register address 10h to high.

3.2.7 Link Test Function

A link pulse is used to check he integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.
The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns

in duration and is transmitted every 16 ms, in the absence of transmit data.

3.2.8 Automatic Link Polarity Detection

ADM6999G's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 5 of register 10h.

3.2.9 Clock Synthesizer

The ADM6999G implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm

3.2.10 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM6999G supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

Highest priority relative to the following list.

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

3.3 Memory Block

ADM6999G build in 768K bits memory inside. Memory buffer is divided as two blocks. One is MAC addressing table and another one is data buffer.

MAC address Learning Table size is 2048 entry with each entry occupy eight bytes length. These eight bytes data include 6 bytes source address, VLAN information, Port information and Aging counter.

Data buffer is divided to 512 bytes/block. ADM6999G buffer management is per port fixed block number and all port share one global buffer. This architecture can get better memory utilization and network balance on different speed and duplex test condition.

Received packet will separate as several 512 bytes/block and chain together. If packet size more than 512 bytes then ADM6999G will chain two or more block to store receiving packet.

3.4 Switch Functional Description

The ADM6999G uses a "store & forward" switching approach for the following reason:
Store & forward switches allow switching between different speed media (e.g. 10BaseX and 100BaseX). Such switches require the large elastic buffer especially bridging between a server on a 100Mbps network and clients on a 10Mbps segment.

Store & forward switches improve overall network performance by acting as a "network cache"

Store & forward switches prevent the forwarding of corrupted packets by the frame check sequence (FCS) before forwarding to the destination port.

3.4.1 Basic Operation

The ADM6999G receives incoming packets from one of its ports, searches in the Address Table for the Destination MAC Address and then forwards the packet to the other port within same VLAN group, if appropriate. If the destination address is not found in the address table, the ADM6999G treats the packet as a broadcast packet and forwards the packet to the other ports which in same VLAN group.

The ADM6999G automatically learns the port number of attached network devices by examining the Source MAC Address of all incoming packets at wire speed. If the Source Address is not found in the Address Table, the device adds it to the table.

3.4.1.1 Address Learning

The ADM6999G uses a hash algorithm to learn the MAC address and can learn up to 2K MAC addresses. Address is stored in the Address Table. The ADM6999G searches for the Source Address (SA) of an incoming packet in the Address Table and acts as below:

If the SA was not found in the Address Table (a new address), the ADM6999G waits until the end of the packet (non-error packet) and updates the Address Table. If the SA was found in the Address Table, then aging value of each corresponding entry will be reset to 0.

When the DA is PAUSE command, then the learning process will be disabled automatically by ADM6999G.

3.4.1.2 Address Recognition and Packet Forwarding

The ADM6999G forwards the incoming packets between bridged ports according to the Destination Address (DA) as below. All the packet forwarding will check VLAN first. Forwarding port must same VLAN with source port.

(1) If the DA is an UNICAST address and the address was found in the Address Table, the ADM6999G will check the port number and acts as follows:

- If the port number is equal to the port on which the packet was received, the packet is discarded.
- If the port number is different, the packet is forwarded across the bridge.

(2) If the DA is an UNICAST address and the address was not found, the ADM6999G treats it as a multicast packet and forwards across the bridge.

(3) If the DA is a Multicast address, the packet is forwarded across the bridge.

(4) If the DA is PAUSE Command (01-80-C2-00-00-01), then this packet will be dropped by ADM6999G. ADM6999G can issue and learn PAUSE command.

(5) ADM6999G will forward the packet with DA of (01-80-C2-00-00-00), filter out the packet with DA of

(01-80-C2-00-00-01), and forward the packet with DA of (01-80-C2-00-00-02 ~ 01-80-C2-00-00-0F)

3.4.1.3 Address Aging

Address aging is supported for topology changes such as an address moving from one port to the other. When this happens, the ADM6999G internally has a 300 seconds timer will aged out (remove) the address from the address table. Aging function can enable/disable by user. Normally, disabling aging function is for security purpose.

3.4.1.4 Back off Algorithm

The ADM6999G implements the truncated exponential back off algorithm compliant to the 802.3 CSMA-CD standard. ADM6999G will restart the back off algorithm by choosing 0-9 collision counts. The ADM6999G resets the collision counter after 16 consecutive retransmit trials.

3.4.1.5 Inter-Packet Gap (IPG)

IPG is the idle time between any two successive packets from the same port. The typical number is 96 bits time. The value is 9.6us for 10Mbps ETHERNET, 960ns for 100Mbps fast ETHERNET and 96ns for 1000M. ADM6999G provide option of 92 bit gap in EEPROM to prevent packet lost when turn off Flow Control and clock P.P.M. value difference.

3.4.1.6 Illegal Frames

The ADM6999G will discard all illegal frames such as runt packet (less than 64 bytes), oversize packet (greater than 1518 or 1522 bytes) and bad CRC. Dribbling packing with good CRC value will accept by ADM6999G. In case of bypass mode enabled, ADM6999G will support tag and untagged packets with size up to 1522 bytes. In case of non-bypass mode, ADM6999G will support tag packets up to 1526bytes, untagged packets up to 1522bytes.

3.4.1.7 Half Duplex Flow Control

Back Pressure function is supported for half-duplex operation. When the ADM6999G cannot allocate a receive buffer for an incoming packet (buffer full), the device will transmit a jam pattern on the port, thus forcing a collision. Back Pressure is enabled by the BPEN set during RESET asserting. An Infineon ADMtek Co Ltd proprietary algorithm is implemented inside the ADM6999G to prevent back pressure function cause HUB partitioned under heavy traffic environment and reduce the packet lost rate to increase the whole system performance.

3.4.1.8 Full Duplex Flow Control

When full duplex port run out of its receive buffer, a PAUSE packet command will be issued by ADM6999G to notice the packet sender to pause transmission. This frame based flow control is totally compliant to IEEE 802.3x. ADM6999G can issue or receive pause packet.

3.4.1.9 Broadcast Storm filter

If Broadcast Storming filter is enable, the broadcast packets over the rising threshold within 50 ms will be discarded by the threshold setting. See EEPROM Reg.10h.

Broadcast storm mode after initial:

- time interval : 50ms

the max. packet number = 7490 in 100Base, 749 in 10Base

Per Port Rising Threshold				
	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

Per Port Falling Threshold				
	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

3.4.2 Auto TP MDIX function

At normal application which Switch connect to NIC card is by one by one TP cable. If Switch connect other device such as another Switch must by two way. First one is Cross Over TP cable. Second way is use extra RJ45 which crossover internal TX+- and RX+- signal. By second way customer can use one by one cable to connect two Switch devices. All these effort need extra cost and not good solution. ADM6999G provide Auto MDIX function which can adjust TX+- and RX+- at correct pin. User can use one by one cable between ADM6999G and other device. This function can be Enable/Disable by hardware pin and EEPROM configuration register 0x01h~0x09h bit 15. If hardware pin set all port at Auto MDIX mode then EEPROM setting is useless. If hardware pin set all port at non Auto MDIX mode then EEPROM can set each port this function enable or disable.

3.4.3 Port Locking

Port locking function will provide customer simple way to limit per port user number to one. If this function is turn on then ADM6999G will lock first MAC address in learning table. After this MAC address locking will never age out except Reset signal. Another MAC address which not same as locking one will be dropped. ADM6999G provide one MAC address per port. This function is per port setting. When turn on Port Locking function, recommend customer turn

off aging function. See EEPROM register 0x12h bit 0~8.

3.4.4 VLAN setting & Tag/Untag & port-base VLAN

ADM6999G supports bypass mode and untagged port as default setting while the chip is power-on. Thus, every packet with or without tag will be forwarding to the destination port without any modification by ADM6999G. Meanwhile port-base VLAN could be enabled according to the PVID value (user define 4bits to map 16 groups written at register 13 to register 22) of the configuration content of each port.

ADM6999G also supports 16 802.1Q VLAN groups. In VLAN four bytes tag include twelve VLAN ID. ADM6999G learn user define four bits of VID. If user need to use this function, two EEPROM registers are needed to be programmed first :

* Port VID number at EEPROM register 0x01h~0x09h bit 13~10, register 0x28h~0x2bh and register 0x2ch bit 7~0: ADM6999G will check coming packet. If coming packet is non VLAN packet then ADM6999G will use PVID as VLAN group reference. ADM6999G will use packet's VLAN value when receive tagged packet.

* VLAN Group Mapping Register. EEPROM register 013h~022h define VLAN grouping value. User use these register to define VLAN group.

User can define each port as Tag port or Untag port by Configuration register Bit 4. The operation of packet between Tag port and Untag port can explain by follow example:

Example1: Port receives Untag packet and send to Untag port.

ADM6999G will check the port user define four bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port then this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

Example2: Port receives Untag packet and send to Tag port.

ADM6999G will check the port user define fours bits of VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port with four byte VLAN Tag and new CRC. If destination port not same VLAN as receiving port then this packet will be dropped.

Example3: Port receives Tag packet and send to Untag port.

ADM6999G will check the packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port after remove four bytes with new CRC error. If destination port not same VLAN as receiving port then this packet will be dropped.

Example4: Port receives Tag packet and send to Tag port.

ADM6999G will check the user define packet VLAN ID first then check VLAN group resister. If destination port same VLAN as receiving port than this packet will forward to destination port without any change. If destination port not same VLAN as receiving port then this packet will be dropped.

3.4.5 Priority Setting

It is a trend that data, voice and video will be put on networking, Switch not only deal data packet but also provide service of multimedia data. ADM6999G provides two priority queues on each port with N:1 rate. See EEPROM Reg.0x10h.

This priority function can set three ways as below:

* By Port Base: Set specific port at specific queue. ADM6999G only check the port priority and not check packet's content VLAN and TOS. ADM6999G only support port base priority at by pass mode.
* By VLAN first: ADM6999G check VLAN three priority bit first then IP TOS priority bits. Chip must set at Tag mode.
* By IP TOS first: ADM6999G check IP TOS three priority bit first then VLAN three priority bits. Chip must set at Tag mode.

If port set at VLAN/TOS priority but receiving packet without VLAN or TOS information then port base priority will be used .

3.4.6 LED Display Interface

The ADM6999G provides three different interfaces to drive the status to the LEDs. Each interface supports visibility per port of port speed, combined transmit and receive activity and duplex collision status. Different interface and it color mode are applied according to LEDMODE pin and the configuration of the ADM6999G latched during the power on reset. Refer to Table 1.3 for an illustration.

Configuration		LEDMODE	Interface utilized
ADM6999G	8+1GMII	1: dual color 0: single color	Serial Interface. Totally two pins, LEDCLK, and LEDDATA are used to output the LED status.

Table 1.3 LED Corresponding Interface

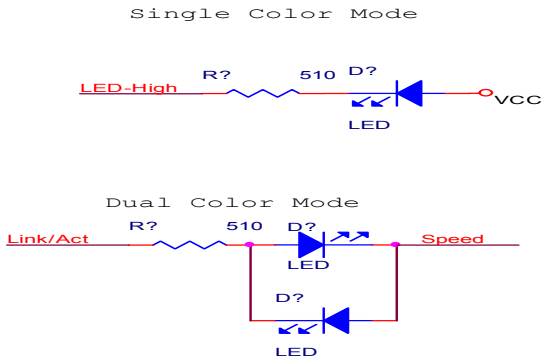
3.4.6.1 Serial LED Interface

A two pins interface, LEDDATA and LEDCLK, provides external shift register to capture the LED status indicated by the ADM6999G. The status is encapsulated within the shift sequence, which is a consecutive stream of 8-bit status words. The first word is the DUPCOL status, the second is the speed status, and the last is the LNKACT status. Each word contains 8 bits and each bit corresponds to each port of the designated LED status. The designated LED status is sent first followed by port1 then port 2, etc. The shift sequence is repeated every 40 ms and each bit last 640ns. Figure 1.2 shows the external circuit.

3.4.6.2 LED Display Mode

Three LED per port are provided by ADM6999G. Link/Act, Duplex/Col & Speed are three LED display of ADM6999G. Dual color LED mode also supported by ADM6999G. For easy production purpose ADM6999G will send test signal to each LED at power on reset stage. EEPROM register 0x12h define LED configuration table.

ADM6999G LED is active Low signal. Dupcol0 & Dupcol1 will check external signal at Reset time. If external signal add pull high then LED will active Low. If external signal add pull down resister then LED will drive high.



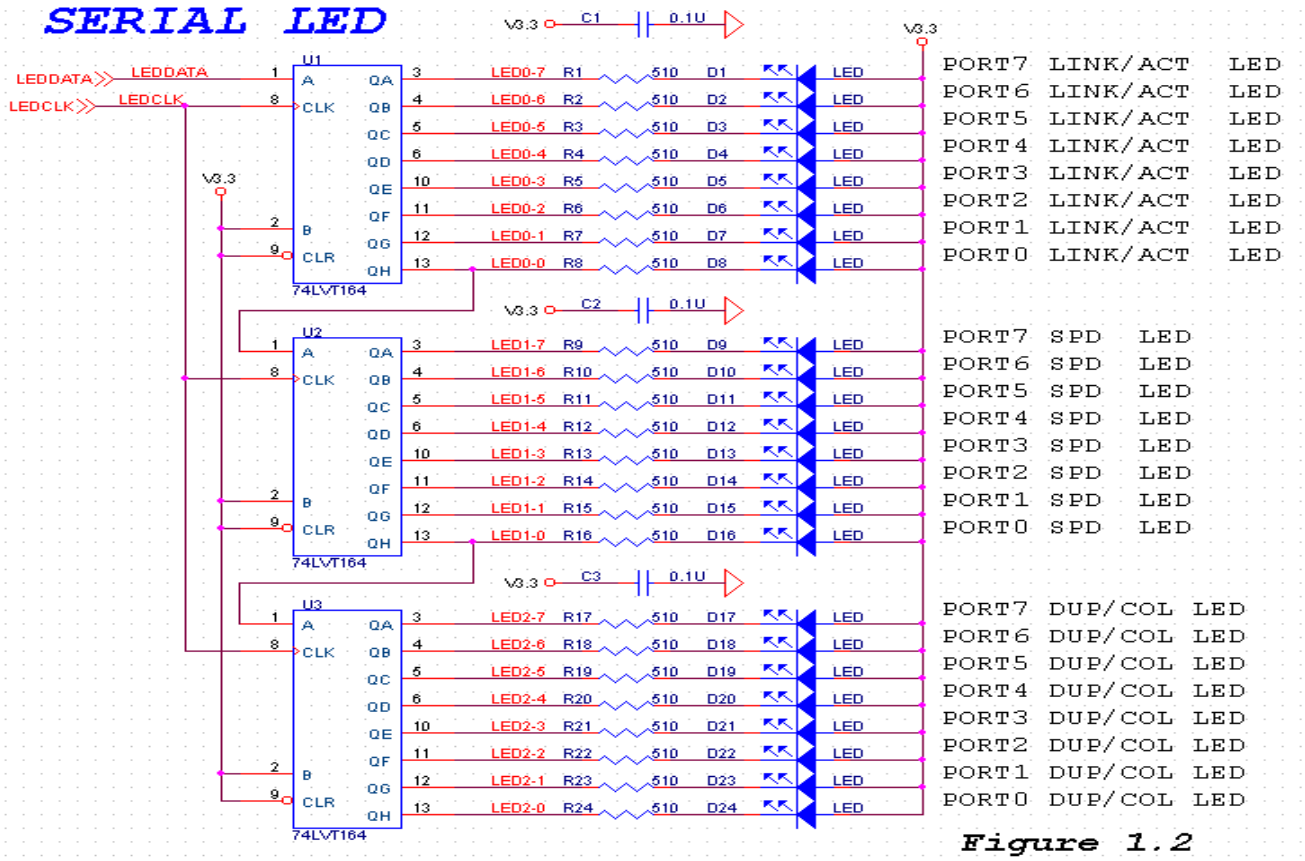


Figure 1.2

3.5 EEPROM Content

EEPROM provides ADM6999G many options setting such as:

* Port Configuration: Speed, Duplex, Flow Control Capability and Tag/ Untag.

* VLAN & TOS Priority Mapping
* Broadcast Storming rate and Trunk.
* Fiber Select, Auto MDIX select
* VLAN Mapping
* Per Port Buffer number

EEPROM Registers

Register	Bit 15- 8	Bit 7 - 0	Default Value
0x00h	Signature	Signature	0x4154h
0x01h	Port 0 Configuration	Port 0 Configuration	0x040fh
0x02h	Port 1 Configuration	Port1 Configuration	0x040fh
0x03h	Port 2 Configuration	Port 2 Configuration	0x040fh
0x04h	Port 3 Configuration	Port 3 Configuration	0x040fh
0x05h	Port 4 Configuration	Port 4 Configuration	0x040fh
0x06h	Port 5 Configuration	Port 5 Configuration	0x040fh
0x07h	Port 6 Configuration	Port 6 Configuration	0x040fh
0x08h	Port 7 Configuration	Port 7 Configuration	0x040fh
0x09h	Port 8 Configuration	Port 8 Configuration	0x040fh
0x0ah	VID 0, 1 option | Giga port Configuration	Giga port Configuration	0x5902h
0x0bh	Configuration Register	Configuration Register	0x8000h
0x0ch	Reserved	Reserved	0xfa50h
0x0dh	Port 8 MII Data High	Port 8 MII Data Low	0xfa50h
0x0eh	VLAN priority Map High	VLAN priority Map Low	0x5500h
0x0fh	TOS priority Map High	TOS priority Map Low	0x5500h
0x10h	Miscellaneous Configuration 0	Miscellaneous Configuration 0	0x0040h
0x11h	Miscellaneous Configuration 1	Miscellaneous Configuration 1	0xff00h
0x12h	Miscellaneous Configuration 2	Miscellaneous Configuration 2	0x3600h
0x13h	VLAN 0 outbound Port Map Or VLAN 1 outbound Port Map	VLAN 0 outbound Port Map Or VLAN 0 outbound Port Map	0xffffh
0x14h	VLAN 1 outbound Port Map Or VLAN 3 outbound Port Map	VLAN 1 outbound Port Map Or VLAN 2 outbound Port Map	0xffffh

0x15h	VLAN 2 outbound Port Map Or VLAN 5 outbound Port Map	VLAN 2 outbound Port Map Or VLAN 4 outbound Port Map	0xffffh
0x16h	VLAN 3 outbound Port Map Or VLAN 7 outbound Port Map	VLAN 3 outbound Port Map Or VLAN 6 outbound Port Map	0xffffh
0x17h	VLAN 4 outbound Port Map Or VLAN 9 outbound Port Map	VLAN 4 outbound Port Map Or VLAN 8 outbound Port Map	0xffffh
0x18h	VLAN 5 outbound Port Map Or VLAN 11 outbound Port Map	VLAN 5 outbound Port Map Or VLAN 10 outbound Port Map	0xffffh
0x19h	VLAN 6 outbound Port Map Or VLAN 13 outbound Port Map	VLAN 6 outbound Port Map Or VLAN 12 outbound Port Map	0xffffh
0x1ah	VLAN 7 outbound Port Map Or VLAN 15 outbound Port Map	VLAN 7 outbound Port Map Or VLAN 14 outbound Port Map	0xffffh
0x1bh	VLAN 8 outbound Port Map Or VLAN 17 outbound Port Map	VLAN 8 outbound Port Map Or VLAN 16 outbound Port Map	0xffffh
0x1ch	VLAN 9 outbound Port Map Or VLAN 19 outbound Port Map	VLAN 9 outbound Port Map Or VLAN 18 outbound Port Map	0xffffh
0x1dh	VLAN 10 outbound Port Map Or VLAN 21 outbound Port Map	VLAN 10 outbound Port Map Or VLAN 20 outbound Port Map	0xffffh
0x1eh	VLAN 11 outbound Port Map Or VLAN 23 outbound Port Map	VLAN 11 outbound Port Map Or VLAN 22 outbound Port Map	0xffffh
0x1fh	VLAN 12 outbound Port Map Or VLAN 25 outbound Port Map	VLAN 12 outbound Port Map Or VLAN 24 outbound Port Map	0xffffh

0x20h	VLAN 13 outbound Port Map Or VLAN 27 outbound Port Map	VLAN 13 outbound Port Map Or VLAN 26 outbound Port Map	0xffffh
0x21h	VLAN 14 outbound Port Map Or VLAN 29 outbound Port Map	VLAN 14 outbound Port Map Or VLAN 28 outbound Port Map	0xffffh
0x22h	VLAN 15 outbound Port Map Or VLAN 31 outbound Port Map	VLAN 15 outbound Port Map Or VLAN 30 outbound Port Map	0xffffh
0x23h	P1 Buffer Threshold Control	P0 Buffer Threshold Control	0x0000h
0x24h	P3 Buffer Threshold Control	P2 Buffer Threshold Control	0x0000h
0x25h	P5 Buffer Threshold Control	P4 Buffer Threshold Control	0x0000h
0x26h	P7 Buffer Threshold Control	P6 Buffer Threshold Control	0x0000h
0x27h	Total Buffer Threshold Control	P8 Buffer Threshold Control	0x0000h
0x28h	P1 PVID [11:4]	P0 PVID [11:4]	0x0000h
0x29h	P3 PVID [11:4]	P2 PVID [11:4]	0x0000h
0x2ah	P5 PVID [11:4]	P4 PVID [11:4]	0x0000h
0x2bh	P7 PVID [11:4]	P6 PVID [11:4]	0x0000h
0x2ch	VLAN Group Configuration	P8 PVID [11:4]	0xd000h
0x2dh	Reserved		0x4442h

Signature Register: 0x00h

Configuration	Description
Bit [15:0]	The value must be 4154h(AT)

ADM6999G will check register 0 value before read all EEPROM content. If this value not match with 0x4154h then other values in EEPROM will be useless. ADM6999G will use internal default value. User can not write Signature register when programming ADM6999G internal register.

Configuration Registers: Register 0x01h ~ 0x09h

Configuration	Description
Bit 0	802.3x Flow control command ability. 1/enable. 0/disable. Default 1.
Bit 1	Auto negotiation Enable. 1/enable, 0/disable. Default 1.
Bit 2	Speed. 1/100M, 0/10M. Default 1.

Bit 3	Duplex. 1/Full Duplex, 0/Half Duplex. Default 1.
Bit 4	Output Packet Tagging. 1/Tag. 0/UnTag. Default 0.
Bit 5	Port Disable. 1/disable port. 0/enable port. Default 0.
Bit 6	TOS over VLAN priority. 1/Check TOS first, 0/Check VLAN. Default 0.
Bit 7	Enable port-base priority. 1/Port Base Priority. 0/VLAN or TOS. If packet without VLAN or TOS then port priority turn on. Default 0.
Bit [9:8]	Port-base priority. Default 00.
Bit [13:10]	PVID. Port VLAN ID. Default 0001.
Bit[14]	Select FX. 1/FX mode. 0/TP mode. Default 0.
Bit [15]	Crossover Auto MDIX enable. 1/enable. 0/disable. Default 0.

Bit 0: 802.3X Flow Control capability. 1: Enable; 0: Disable.

Bit 1: Auto Negotiation capability Enable. 1: Enable; 0: Disable.

Bit 2: Speed Capability. 1: 100, 0: 10.

Bit 3: Duplex Capability. 1: Full, 0: Half.

Bit 4: VLAN Tag Port. 1: Tag port; 0: Untag port.

Bit 5: Port Disable. 1/disable port, 0/enable port. This function not include Port8. Port8 disable can be done by VLAN separation.

Bit 6: TOS over VLAN Priority. Define ADM6999G priority source when VLAN & TOS existed in the packet. 1: TOS priority level higher than VLAN, 0: VLAN priority level higher than TOS.

Bit 7: Enable Port Based Priority. 1: Enable, 0: Disable. If this bit turn on then ADM6999G will not check TOS or VLAN as priority reference. ADM6999G will check port base priority only. ADM6999G default is bypass mode which checks port base priority only. If user want check VLAN tag priority then must set chip at Tag mode. See 0x11h.

Bit[9:8]: Port base priority number. From 1~0 mapping to Q1~Q0.

Bit[13:10]: Port VLAN ID bit[3:0]. Check Register 0x28h~0x2ch for other PVID[11:4].

Bit[14]: Select FX interface. 1: FX, 0: TP. Port7 TX/FX can set by hardware Reset latch value P7FX. If hardware pin set Port7 as FX then this bit is useless. If hardware pin set Port7 as TX then this pin can set Port7 as FX or TX.

Bit[15]: Auto MDIX enable. 1: Enable, 0: Disable. Hardware Reset latch value EECK can set global Auto MDIX function. If hardware pin set all port at Auto MDIX then this bit is useless. If hardware pin set chip at non Auto MDIX then this bit can set each port at Auto MDIX.

Note: Register 0x09h bit5 is not effective on disable port. User can disable port by VLAN.

Register 0x0ah: Gigabit Port Configuration Register.

Configuration	Description

Bit [7:0]	MII register 9 bit[15:8]. Default 0x20h.
Bit 8	Giga Speed selection MSB. MII register 0x01h. Default 1.
Bit 9	Replaced packet VID 0, 1 by PVID. 1/ enable, 0/disable. Default 0.
Bit [15:10]	Reserved. Default 010110.

Bit[7~0]: MII register 0x09h bit[15~8]. See MII register 0x09h definition.

Bit 8: Gigabit Speed selection MSB bit of MII register 0x01h.

Bit 9: Replaced VID 0, 1. 1/ADM6999G will replace packet VID by PVID when coming packet's VID=0 or1, 0/ADM6999G will not replace packet's VID 0 & 1.

Configuration Register: Register 0x0bh

Configuration	Description
Bit [4:0]	Reserved. Default 00000.
Bit 5	Reserved. Default 0.
Bit 6	Enable IPG leveling. 1/92 bit. 0/96 bit. Default 0.
Bit 7	Enable Trunk. 1/enable Port6, 7 as Trunk port. 0/disable. Default 0.
Bit [12:8]	Port 8 MII Register Address. Default 00000.
Bit 13	Port 8 MII Write Enable. High Active. Default 0.
Bit 14	Reserved. Default 0.
Bit 15	Disable Far_End_Fault detection. 1/disable. 0/enable. Default 1.

Bit 6: Enable IPG Leveling. 1/Enable. 0/Disable. When this bit is enable ADM6999G will transmit packet out at 96 bit or 92 bit to clean buffer. If user disable this function then ADM6999G will transmit packet at 96 bit.

Bit 7: Enable Trunk. 1/Enable Port6 & 7 as Trunk Port. 0/Disable.

Bit [12:8]: Port 8 MII register address. If user want write data to Port8's PHY through MDC/MDIO then these five bits can give MII register address.

Bit 13: Port8 MII register write enable. 1/enable write. 0/disable.

Bit 15: Disable Far_End_Fault detection. 1/disable. 0/enable. Default 1. ADM6999G will not recognize Far_End_Fault when turn on this bit.

Register 0x0ch: Reserved.

Configuration	Description
Bit [15:0]	Reserved.

Register 0x0dh: Port 8 MII write data

Configuration	Description
Bit [15:0]	Port8 MII register write data.

Bit[15:0]: User can fill out write data for specific port8 MII register as assigned in register 0x0bh.

Register 0x0eh: VLAN priority Map.

Configuration	Description
Bit [1:0]	Mapped priority of tag value(VLAN) 0. Default 0.
Bit [3:2]	Mapped priority of tag value(VLAN) 1. Default 0.
Bit [5:4]	Mapped priority of tag value(VLAN) 2. Default 0.
Bit [7:6]	Mapped priority of tag value(VLAN) 3. Default 0.
Bit [9:8]	Mapped priority of tag value(VLAN) 4. Default 1.
Bit [11:10]	Mapped priority of tag value(VLAN) 5. Default 1.
Bit [13:12]	Mapped priority of tag value(VLAN) 6. Default 1.
Bit [15:14]	Mapped priority of tag value(VLAN) 7. Default 1.

00: low priority queue. Q0

01: high priority queue. Q1

The weight ratio is 1:N. Queue ratio(defined in 0x10h bit[13:12])

Reg. 0x10 Bit[13:12]	Weight radio
00	1:1
01	1:2
10	1:3
11	1:4

The default is port-base priority for un-tag packet and none IP frame.

Register 0x0fh: TOS priority Map.

Configuration	Description
Bit [1:0]	Mapped priority of tag value(TOS) 0. Default 0.
Bit [3:2]	Mapped priority of tag value(TOS) 1. Default 0.
Bit [5:4]	Mapped priority of tag value(TOS) 2. Default 0.
Bit [7:6]	Mapped priority of tag value(TOS) 3. Default 0.
Bit [9:8]	Mapped priority of tag value(TOS) 4. Default 1.
Bit [11:10]	Mapped priority of tag value(TOS) 5. Default 1.

Bit [13:12]	Mapped priority of tag value(TOS) 6. Default 1.
Bit [15:14]	Mapped priority of tag value(TOS) 7. Default 1.

00: low priority queue. Q0

01: high priority queue. Q1

The weight ratio is 1:N. Queue ratio(defined in 0x10h/bit[13:12])

Reg. 0x10 Bit[13:12]	Weight radio
00	1:1
01	1:2
10	1:3
11	1:4

The default is port-base priority for un-tag packet and none IP frame.

Packet with Priority:

Normal packet content

Ethernet Packet from Layer 2

Preamble/SFD	Destination (6 bytes)	Source (6 bytes)	Packet length (2 bytes)	Data (46-1500 bytes)	CRC (4 bytes)
	Byte 0~5	Byte 6~11	Byte 12~13	Byte 14~	

VLAN Packet

ADM6999G will check packet byte 12 &13. If byte[12:13]=8100h then this packet is a VLAN packet

Tag Protocol TD 8100	Tag Control Information TCI	LEN Length	Routing Information
Byte 12~13	Byte14~15	Byte 16~17	Byte 18

Byte 14~15: Tag Control Information TCI

Bit[15:13]: User Priority 7~0

Bit 12: Canonical Format Indicator (CFI)

Bit[11~0]: VLAN ID. The ADM6999G will use bit[3:0] as VLAN group.

TOS IP Packet

ADM6999G check byte 12 &13 if this value is 0800h then ADM6999G knows this is a TOS priority packet.

Type 0800	IP Header
Byte 12~13	Byte 14~15

IP header define

Byte 14

Bit[7:0]: IP protocol version number & header length.

Byte 15: Service type

Bit[7~5]: IP Priority (Precedence) from 7~0

Bit 4: No Delay (D)

Bit 3: High Throughput

Bit 2: High Reliability (R)

Bit[1:0]: Reserved

Miscellaneous Configuration: Register 0x10h

Configuration	Description
Bit [1:0]	Broadcast Storming Threshold[1:0]. See below table. Default 00.
Bit [2]	Broadcast Storming Enable. 1/ enable, 0/disable. Default 0.
Bit [3]	Reserved. Default 0.
Bit [4]	XCRC. 1/disable CRC check, 0/enable CRC Check. Default 0.
Bit [5]	Reserved. Default 0.
Bit [6]	Reserved. Default 0.
Bit [7]	Aging Disable. 1/disable aging, 0/enable aging. Default 0.
Bit [9:8]	Discard mode (drop scheme for Q0)
Bit [11:10]	Discard mode (drop scheme for Q1)
Bit [13:12]	Queue ratio 00 : 1:1 01 : 1:2 10 : 1:3 11 : 1:4
Bit [15:14]	Reserved

Bit[1:0]: Broadcast Storming threshold.

Broadcast storm mode after initial:

- time interval : 50ms

the max. packet number = 7490 in 100Base, 749 in 10Base

- per port rising threshold

	00	01	10	11
All 100TX	Disable	10%	20%	40%
Not All 100TX	Disable	1%	2%	4%

- per port falling threshold

	00	01	10	11
All 100TX	Disable	5%	10%	20%
Not All 100TX	Disable	0.5%	1%	2%

Bit 2: Broadcast Storming Enable. 0/Disable. 1/Enable.

Bit 4: CRC check disable. 1/ Disable. 0/Enable.

Bit 7: Aging Disable. 1/Disable. 0/Enable.

- Drop Scheme for each queue

Discard Mode / Utilization	00	01	10	11
TBD	0%	0%	25%	50%

Register 0x11h: VLAN mode select Register.

Configuration	Description
Bit [3:0]	Reserved, default value 0000
Bit [4]	MAC Clone enable, default 0 0 : Normal mode. Learning with SA only. 1: MAC Clone mode. Learning with SA, VID0.
Bit [5]	VLAN mode select, default 0 0 : by-pass mode with port-base VLAN. 1 : 802.1Q base VLAN.
Bit [7:6]	Reserved. Default value 00
Bit [8]	Reserved. Default 1.
Bit [9]	Reserved. Default 1.
Bit [10]	Back-pressure enable, 1/ enable. 0/disable. Default value is 1

Bit [15:11]	Reserved, default value 11111.

Bit 4: MAC Clone enable.

0 : Normal mode. Learning with SA only. ADM6999G fill/search MAC table by SA or DA only.

1: MAC Clone mode. Learning with SA, VID0. ADM6999G fill/search MAC table by SA or DA with VID0. This bit can let chip learn two same addresses with different VID0.

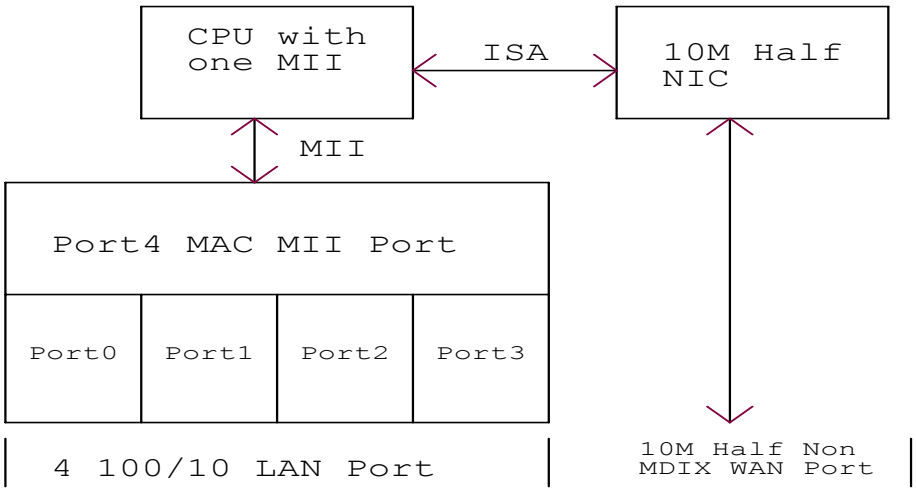
Bit 5: VLAN mode select, default is 0. 0/By-pass mode with port-base VLAN. 1/802.1Q base VLAN.

Bit 10: Back Pressure Enable. 1/enable, 0/disable. This is a global pin for all ports.

Below is Bit4, 5 VLAN Tag and MAC application example base on Infineon ADMtek Co Ltd ADM6996.

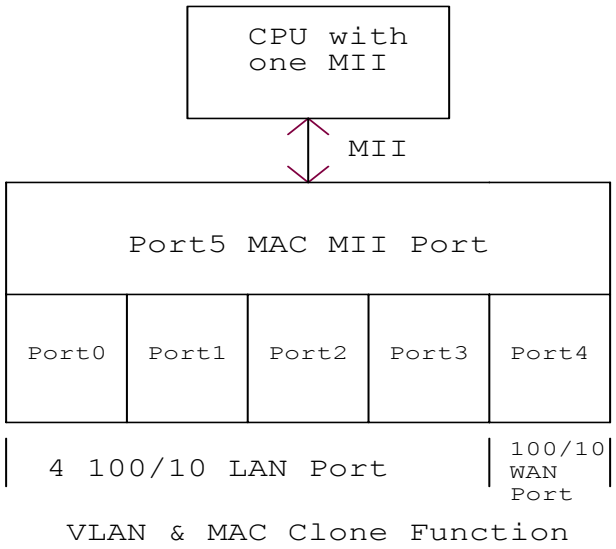
Below is Router old architecture. The disadvantages of this are:

1. WAN port only support 10M Half-Duplex and non-MDIX function.
2. Need extra 10M NIC cost.
3. ISA bus will become bottleneck of whole system.



Below is new architecture by using ADM6999 serial chip VLAN function. The advantages of below are:

1. WAN Port can upgrade to 100/10 Full/Half , Auto MDIX.
2. WAN/LAN Port is programmable and put on same Switch.
3. No need extra NIC and save lot of cost.
4. High bandwidth of MII port up to 200M speed.



New Router application works well on normal application. If user's ISP vendor(cable modem) lock Registration Card's ID then Router CPU must send this Lock Registration Card's ID to WAN Port. One condition happen is there exist two same MAC ID on this Switch. One is original Card and another one is CPU. This will make Switch learning table trouble.

ADM6999 provide MAC Clone function that allow two same MAC address with different VLAN ID0 on learning table. This will solve Lock registration Card's ID issue. ADM6999 serial chips will put these two same MAC addresses with different VLAN ID0 at different learning table entry.

How to Set ADM6999 on Router.

Port0~3: LAN Port.

Port4: WAN Port.

Port5: MII Port as CPU Port.

Step1: Set Register 0x11h bit4 and bit5 to 1.

{Coding: Write Register 0x11h as 0xff30h}

Step2: Set Port0~3 as Untag Port and set PVID=1.

{ Coding: Write Register 0x01h, 0x03h, 0x05h, 0x07h as 0x840f. Port0~3 as Untag, PVID=1, Enable MDIX}

Step3: Set Port4 as Untag Port and set PVID=2.

{ Coding: Write Register 0x08h as 0x880fh. Port4 as Untag, PVID=2, Enable MDIX.}

Step4: Set Port5 MII Port as Tag Port and set PVID=2.

{ Coding: Write Register 0x09h as 0x881fh. Port5 MII port as Tag, PVID=2.}

Step5: Group Port0, 1, 2, 3, 5 as VLAN 1.

{ Coding: Write Register 0x14h as 0x0155h. VLAN1 cover Port0, 1, 2, 3, 5.}

Step6: Group Port4, 5 as VLAN 2.

{ Coding: Write Register 0x15h as 0x0180h. VLAN2 cover Port4, 5.}

How MAC Clone Operation:

1. LAN to LAN/CPU Traffic.

   ADM6999 LAN traffic to LAN/CPU only. Traffic to another LAN port will be untag packet. Traffic to CPU is Tag packet with VID=1. CPU can check VID to distinguish LAN traffic or WAN traffic.

2. WAN to CPU Traffic.

   ADM6999 WAN traffic to CPU only. Traffic to CPU is Tag packet with VID=2. CPU can check VID to distinguish LAN traffic or WAN traffic.

3. CPU to LAN Packet.

   ADM6999 CPU Packet to LAN port must add VID=1 in VLAN field. AT8995 check VID to distinguish LAN traffic or WAN traffic. LAN output packet is Untag.

4. CPU to WAN Packet.

   ADM6999 CPU Packet to WAN port must add VID=2 in VLAN filed. AT8995 check VID to distinguish LAN traffic or WAN traffic. WAN output packet is Untag.

5. ADM6999 learning sequence

   ADM6999 will check VLAN mapping setting first then check learning table. User does not worry LAN/WAN traffic mix up.

Bit 10: Half Duplex Back Pressure enable. 1/enable, 0/disable.

Register 0x12h: Miscellaneous Configuration register.

Configuration	Description
Bit [0]	Port0 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.
Bit [1]	Port1 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.
Bit [2]	Port2 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.
Bit [3]	Port3 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.
Bit [4]	Port4 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.
Bit [5]	Port5 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.
Bit [6]	Port6 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.
Bit [7]	Port7 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.

Bit [8]	Port8 MAC Lock. 1/Lock first MAC source address, 0/disable. Default 0.
Bit [10:9]	Reserved
Bit [11]	Reserved
Bit [13:12]	Power Saving Select
Bit [14]	Reserved
Bit [15]	Drop packet when excessive collision happen enable. 1/ enable, 0/disable. Default 0.

Bit [8:0]: Port Locking enable. Learn one MAC ID when enable. 1/enable. 0/disable.

Bit[15]: Half Duplex excessive collision(16) drop packet enable. 1/drop. 0/no drop.

Register 0x22h~ 0x13h: VLAN mapping table registers.

16 VLAN Group: See Register 0x2ch bit 11=0

Configuration	Description
Bit [8:0]	VLAN mapping table.

Bit0: Port0 Bit1: Port1 Bit2: Port2 Bit3: Port3

Bit4: Port4 Bit5: Port5 Bit6: Port6 Bit7: Port7

Bit8: Port8.

Select the VLAN group ports is to set the corresponding bits to 1.

32 VLAN Group: See Register 0x2ch bit 11=1

Configuration	Description
Odd VLAN mapping table	Even VLAN mapping table

Bit0, 8: Port0 Bit1, 9: Port1 Bit2, 10: Port2 Bit3, 11: Port3

Bit4, 12: Port4 Bit5, 13: Port5 Bit6, 14: Port6 Bit7, 15: Port7

All VLAN groups will cover Port8 at 32 group mode. This feature is good for multiple ADM6999G systems.

Register 0x26h~0x23h: Per Port Buffer Threshold Control.

Configuration	Description
Bit [7:0]	Even Port Buffer Threshold Control
Bit [15:8]	Odd Port Buffer Threshold Control

Bit [7:0] : Buffer threshold control for even port

Bit [15:8] : Buffer threshold control for odd port

Reg.23 Bit [7:0] : port0 Reg.23 Bit [15:8] : port1 Reg.24 Bit [7:0] : port2 Reg.24 Bit [15:8] : port3

Reg.25 Bit [7:0] : port4 Reg.25 Bit [15:8] : port5 Reg.26 Bit [7:0] : port6 Reg.26 Bit [15:8] : port7

ADM6999G supports buffer management scheme with dynamic thresholds to ensure the fair share of memory among different port queues. If users need each port to have a fixed threshold, they can configure the Bit 14 in the 0x27h to 1.

Dynamic threshold management:

Bit[7]: The add bit. Bit[6:0]: The offset bits.

When Bit[7] = 1, the switch will use the value (buffers really used + 2*bit[6:0]) as the buffer count that the port has used.

When Bit[7] = 0, the switch will use the value (buffers really used - 2*bit[6:0]) as the buffer count that the port has used.

Fixed threshold management:

Bit[3:0]: The buffer threshold bits.

When the total buffer was not reached, the buffer amount allocated to each port will be equal to bit[3:0] * 4.

0x27h: Total Buffer Threshold Control.

Configuration	Description
Bit [7:0]	Port8 Buffer Threshold Control.
Bit [13:8]	Total Buffer Threshold Control
Bit[14]	Reserved. Default 0.
Bit[15]	Reserved. Default 0.

Bit [7:0] : Port8 Buffer Threshold Control. The configuration is the same as the other ports.

Bit [13:8] : Total buffer Threshold control.

Dynamic threshold management:

Bit[13]: The add bit. Bit[12:8]: The offset bits.

When Bit[13] = 1, the switch will use the value (buffers really used + 8*bit[12:8]) as the buffer count that the switch has used.

When Bit[13] = 0, the switch will use the value (buffers really used - 8*bit[12:8]) as the buffer count that the switch has used.

Fixed threshold management:

Bit[13]: This bit doesn't affect the threshold.

Bit[12:8]: The total buffer threshold bits.

0x28h: Port0, 1 PVID bit 11~4 Configuration Register.

Configuration	Description

Bit [7:0]	Port0 PVID bit 11~4. These 8 bits combine with register 0x01h Bit[13~10] as full 12 bit VID. Default 0x00h.
Bit [15:8]	Port1 PVID bit 11~4. These 8 bits combine with register 0x02h Bit[13~10] as full 12 bit VID. Default 0x00h.

0x29h: Port2, 3 PVID bit 11~4 Configuration Register.

Configuration	Description
Bit [7:0]	Port2 PVID bit 11~4. These 8 bits combine with register 0x03h Bit[13~10] as full 12 bit VID. Default 0x00h.
Bit [15:8]	Port3 PVID bit 11~4. These 8 bits combine with register 0x04h Bit[13~10] as full 12 bit VID. Default 0x00h.

0x2ah: Port4, 5 PVID bit 11~4 Configuration Register.

Configuration	Description
Bit [7:0]	Port4 PVID bit 11~4. These 8 bits combine with register 0x05h Bit[13~10] as full 12 bit VID. Default 0x00h.
Bit [15:8]	Port5 PVID bit 11~4. These 8 bits combine with register 0x06h Bit[13~10] as full 12 bit VID. Default 0x00h.

0x2bh: Port6, 7 PVID bit 11~4 Configuration Register.

Configuration	Description
Bit [7:0]	Port6 PVID bit 11~4. These 8 bits combine with register 0x07h Bit[13~10] as full 12 bit VID. Default 0x00h.
Bit [15:8]	Port7 PVID bit 11~4. These 8 bits combine with register 0x08h Bit[13~10] as full 12 bit VID. Default 0x00h.

0x2ch: Port8 PVID bit 11~4 and VLAN group shift bits Configuration Register.

Configuration	Description
Bit [7:0]	Port8 PVID bit 11~4. These 8 bits combine with register 0x09h Bit[13~10] as full 12 bit VID. Default 0x00h.
Bit [10:8]	Tag shift for VLAN grouping. Default 000. **16 VLAN Mode** 0: VID[3:0] 1: VID[4:1] 2: VID[5:2]

<table>
<tr><td></td><td colspan="2">3: VID[6:3] 4: VID[7:4] 5: VID[8:5]
6: VID[9:6] 7: VID[10:7]

32 VLAN Mode
0: VID[4:0] 1: VID[5:1] 2: VID[6:2]
3: VID[7:3] 4: VID[8:4] 5: VID[9:5]
6: VID[10:6] 7: VID[11:7]</td></tr>
<tr><td>Bit [11]</td><td colspan="2">VLAN Mode. 1/32 VLAN group, 0/16 VLAN group. Default 0.</td></tr>
<tr><td rowspan="5">Bit [15:12]</td><td colspan="2">Special address forwarding : default is 1101</td></tr>
<tr><td>Bit[15]</td><td>Control reserved MAC (0180C2000010-0180C20000FF)
1: Forward, 0: Discard. Default: 1.</td></tr>
<tr><td>Bit[14]</td><td>Control reserved MAC (0180C2000002-0180C200000F)
1: Forward, 0: Discard. Default: 1.</td></tr>
<tr><td>Bit[13]</td><td>Control reserved MAC (0180C2000001)
1: Forward, 0: Discard. Default: 0.</td></tr>
<tr><td>Bit[12]</td><td>Control reserved MAC (0180C2000000)
1: Forward, 0: Discard. Default: 1.</td></tr>
</table>

Bit[10:8]: VLAN Tag shift register. ADM6999G will select 4/5 bit from total 12 bit VID as VLAN group reference. Select 4 or 5 bit from VID depend on bit 11 setting. For example Bit[10:8]=001, Bit11=0, then ADM6999G will select packet VID4~VID1 as VLAN group mapping. It is very flexible for user on VLAN grouping.

Bit[11]: VLAN mode. Select 16 or 32 VLAN group.

Bit[15:12]: IEEE 802.3 reserved DA forward or drop police.

3.6 EEPROM Access

Customer can select ADM6999G read EEPROM contents as chip setting or not. ADM6999G will check the signature of

EEPROM to decide read content of EEPROM or not.

RC & EEPROM content relationship

RC	CS	SK	DI	DO

0	High Impedance	High Impedance	High Impedance	High Impedance
Rising edge 0→1 (30ms)	Output	Output	Output	Input
1 (after 30ms)	Input	Input	I/O	Input

Keep at least 30ms after RC from 0→1. ADM6999G will read data from EEPROM. After RC if CPU update EEPROM that ADM6999G will update configuration registers too.

When CPU programming EEPROM & AT8995, ADM6999G recognizes the EEPROM WRITE instruction only. If there is any Protection instruction before or after the EEPROM WRITE instruction, CPU needs to generate separated CS signal cycle for each Protection & WRITE instruction.

CPU can directly program ADM6999G after 30ms of Reset signal rising edge with or without EEPROM

ADM6999G serial chips will latch hardware-reset value as recommend value. It includes EEPROM interface:

EECS: Internal Pull down 40K resister.

EESK: TP port Auto-MDIX select. Internal pull down 40K resister as non Auto-MDIX mode.

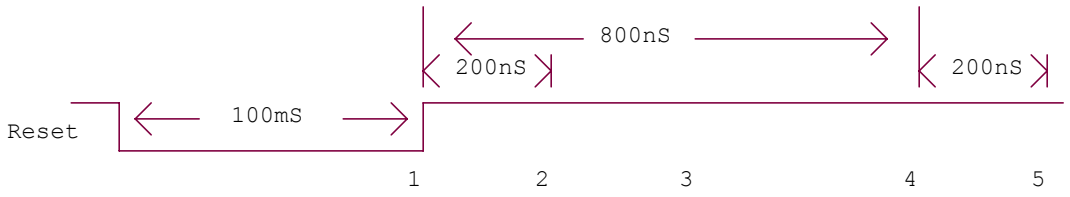
EDI: Dual Color Select. Internal pull down 40K resister as Single Color Mode.

EDO: EEPROM enable. Internal pull up 40K resister as EEPROM enable.

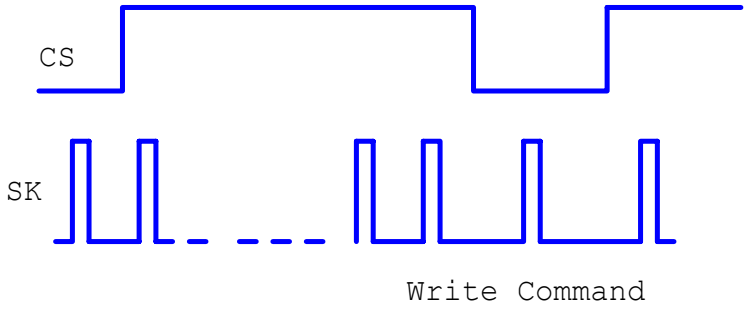
Below Figure is ADM6999G serial chips EEPROM pins operation at different stage. Reset signal is control by CPU with at least 100ms low. Point1 is Reset rising edge. CPU must prepare proper value on ECS(0), EESK, EDI, EDO(1) before this rising edge. ADM6999G will read this value into chip at Point2. CPU must keep these values over point2. Point2 is 200ns after Reset rising edge.

ADM6999G serial chips will read EEPROM content at Point4 which 800ns far away from the rising edge of Reset. CPU must turn EEPROM pins EECS, EESK, EDI and EDO to High-Z or pull high before Point4.

If user want change state to High-Z or pull high on EEPROM pins, the order is CS-> DI -> DO -> SK is better.



A little bit different with the timing on writing EEPROM. See below graph. Must be carefully is when CS go down after write a command, SK must issue at least one clock. This is a difference between ADM6999G with EEPROM write timing. If system without EEPROM then user must write ADM6999G internal register by 93C66 timing. If user uses EEPROM then the writing timing is depend on EEPROM type.


CS
SK
Write Command

4. Serial Management

Serial Registers Map.

RO: Read Only

LH/COR: Read and Clear.

Register	Bit 31- 0	MODE	Default
0x00h	Chip Identifier	RO	0x00021120h
0x01h	Port Status 0	RO	0x00000000h
0x02h	Port Status 1	RO	0x00000000h
0x03h	Cable Broken Status	RO	0x00000000h
0x04h	Port 0 Receive Packet Count	RO	0x00000000h
0x05h	Port 1 Receive Packet Count	RO	0x00000000h
0x06h	Port 2 Receive Packet Count	RO	0x00000000h
0x07h	Port 3 Receive Packet Count	RO	0x00000000h
0x08h	Port 4 Receive Packet Count	RO	0x00000000h
0x09h	Port 5 Receive Packet Count	RO	0x00000000h
0x0ah	Port 6 Receive Packet Count	RO	0x00000000h
0x0bh	Port 7 Receive Packet Count	RO	0x00000000h
0x0ch	Port 8 Receive Packet Count	RO	0x00000000h
0x0dh	Port 0 Receive Packet Byte Count	RO	0x00000000h
0x0eh	Port 1 Receive Packet Byte Count	RO	0x00000000h
0x0fh	Port 2 Receive Packet Byte Count	RO	0x00000000h
0x10h	Port 3 Receive Packet Byte Count	RO	0x00000000h
0x11h	Port 4 Receive Packet Byte Count	RO	0x00000000h
0x12h	Port 5 Receive Packet Byte Count	RO	0x00000000h
0x13h	Port 6 Receive Packet Byte Count	RO	0x00000000h
0x14h	Port 7 Receive Packet Byte Count	RO	0x00000000h
0x15h	Port 8 Receive Packet Byte Count	RO	0x00000000h
0x16h	Port 0 Transmit Packet Count	RO	0x00000000h
0x17h	Port 1 Transmit Packet Count	RO	0x00000000h
0x18h	Port 2 Transmit Packet Count	RO	0x00000000h
0x19h	Port 3 Transmit Packet Count	RO	0x00000000h
0x1ah	Port 4 Transmit Packet Count	RO	0x00000000h

0x1bh	Port 5 Transmit Packet Count	RO	0x00000000h
0x1ch	Port 6 Transmit Packet Count	RO	0x00000000h
0x1dh	Port 7 Transmit Packet Count	RO	0x00000000h
0x1eh	Port 8 Transmit Packet Count	RO	0x00000000h
0x1fh	Port 0 Transmit Packet Byte Count	RO	0x00000000h
0x20h	Port 1 Transmit Packet Byte Count	RO	0x00000000h
0x21h	Port 2 Transmit Packet Byte Count	RO	0x00000000h
0x22h	Port 3 Transmit Packet Byte Count	RO	0x00000000h
0x23h	Port 4 Transmit Packet Byte Count	RO	0x00000000h
0x24h	Port 5 Transmit Packet Byte Count	RO	0x00000000h
0x25h	Port 6 Transmit Packet Byte Count	RO	0x00000000h
0x26h	Port 7 Transmit Packet Byte Count	RO	0x00000000h
0x27h	Port 8 Transmit Packet Byte Count	RO	0x00000000h
0x28h	Port 0 Collision Count	RO	0x00000000h
0x29h	Port 1 Collision Count	RO	0x00000000h
0x2ah	Port 2 Collision Count	RO	0x00000000h
0x2bh	Port 3 Collision Count	RO	0x00000000h
0x2ch	Port 4 Collision Count	RO	0x00000000h
0x2dh	Port 5 Collision Count	RO	0x00000000h
0x2eh	Port 6 Collision Count	RO	0x00000000h
0x2fh	Port 7 Collision Count	RO	0x00000000h
0x30h	Port 8 Collision Count	RO	0x00000000h
0x31h	Port 0 Error Count	RO	0x00000000h
0x32h	Port 1 Error Count	RO	0x00000000h
0x33h	Port 2 Error Count	RO	0x00000000h
0x34h	Port 3 Error Count	RO	0x00000000h
0x35h	Port 4 Error Count	RO	0x00000000h
0x36h	Port 5 Error Count	RO	0x00000000h
0x37h	Port 6 Error Count	RO	0x00000000h
0x38h	Port 7 Error Count	RO	0x00000000h
0x39h	Port 8 Error Count	RO	0x00000000h
0x3ah	Over Flow Flag 0	LH/COR	0x00000000h
0x3bh	Over Flow Flag 1	LH/COR	0x00000000h

0x3ch	Over Flow Flag 2	LH/COR	0x00000000h

Chip Identifier: Register 0x00h

Configuration	Description
Bit [3:0]	0000(Version number)
Bit [31:4]	0x0002112h

Port Status 0: Register 0x01h

Configuration	Description
Bit[0]	Port 0 Linkup Status: 1: Link is established. 0: Link is not established.
Bit[1]	Port 0 Speed Status: 1: 100Mb/s 0: 10 Mb/s
Bit[2]	Port 0 Duplex Status 1: Full Duplex. 0: Half Duplex.
Bit[3]	Port 0 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable
Bit[4]	Port 1 Linkup Status: 1: Link is established. 0: Link is not established.
Bit[5]	Port 1 Speed Status: 1: 100Mb/s 0: 10 Mb/s
Bit[6]	Port 1 Duplex Status 1: Full Duplex. 0: Half Duplex.
Bit[7]	Port 1 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable
Bit[8]	Port 2 Linkup Status: 1: Link is established. 0: Link is not established.
Bit[9]	Port 2 Speed Status: 1: 100Mb/s 0: 10 Mb/s
Bit[10]	Port 2 Duplex Status 1: Full Duplex.

	0: Half Duplex.
Bit[11]	Port 2 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable
Bit[12]	Port 3 Linkup Status: 1: Link is established. 0: Link is not established.
Bit[13]	Port 3 Speed Status: 1: 100Mb/s 0: 10 Mb/s
Bit[14]	Port 3 Duplex Status 1: Full Duplex. 0: Half Duplex.
Bit[15]	Port 3 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable
Bit[16]	Port 4 Linkup Status: 1: Link is established. 0: Link is not established.
Bit[17]	Port 4 Speed Status: 1: 100Mb/s 0: 10 Mb/s
Bit[18]	Port 4 Duplex Status 1: Full Duplex. 0: Half Duplex.
Bit[19]	Port 4 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable
Bit[20]	Port 5 Linkup Status: 1: Link is established. 0: Link is not established.
Bit[21]	Port 5 Speed Status: 1: 100Mb/s 0: 10 Mb/s
Bit[22]	Port 5 Duplex Status 1: Full Duplex. 0: Half Duplex.
Bit[23]	Port 5 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable
Bit[24]	Port 6 Linkup Status: 1: Link is established. 0: Link is not established.

Bit[25]	Port 6 Speed Status: 1: 100Mb/s 0: 10 Mb/s
Bit[26]	Port 6 Duplex Status 1: Full Duplex. 0: Half Duplex.
Bit[27]	Port 6 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable
Bit[28]	Port 7 Linkup Status: 1: Link is established. 0: Link is not established.
Bit[29]	Port 7 Speed Status: 1: 100Mb/s 0: 10 Mb/s
Bit[31]	Port 7 Duplex Status 1: Full Duplex. 0: Half Duplex.
Bit[31]	Port 7 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable

Port Status 1: Register 0x02h

Configuration	Description
Bit [0]	Port 8 Linkup Status: 1: Link is established. 0: Link is not established.
Bit [2:1]	Port 8 Speed Status: Two bits indicate the operating speed. Bit[2] Bit[1] Speed 1 x 1000Mb/s 0 1 100Mb/s 0 0 10Mb/s
Bit [3]	Port 8 Duplex Status 1: Full Duplex. 0: Half Duplex.
Bit [4]	Port 8 Flow Control Enable 1: 802.3X on for full duplex or back pressure on for half duplex. 0: Flow Control Disable
Bit [31:5]	Reserved. Default is 0h.

Cable Broken Status: Register 0x03h

Configuration	Description
Bit [1:0]	Port 0 Cable Broken Length
Bit[2]	Port 0 Cable Broken
Bit [4:3]	Port 1 Cable Broken Length
Bit[5]	Port 1 Cable Broken
Bit [7:6]	Port 2 Cable Broken Length
Bit[8]	Port 2 Cable Broken
Bit [10:9]	Port 3 Cable Broken Length
Bit[11]	Port 3 Cable Broken
Bit [13:12]	Port 4 Cable Broken Length
Bit[14]	Port 4 Cable Broken
Bit [16:15]	Port 5 Cable Broken Length
Bit[17]	Port 5 Cable Broken
Bit [19:18]	Port 6 Cable Broken Length
Bit[20]	Port 6 Cable Broken
Bit [22:21]	Port 7 Cable Broken Length
Bit[23]	Port 7 Cable Broken
Bit [31:24]	Reserved. Default is 0h.

Over Flow Flag 0: Register 0x3ah

Configuration	Description
Bit [0]	Overflow of Port 0 Receive Packet Count
Bit [1]	Overflow of Port 1 Receive Packet Count
Bit [2]	Overflow of Port 2 Receive Packet Count
Bit [3]	Overflow of Port 3 Receive Packet Count
Bit [4]	Overflow of Port 4 Receive Packet Count
Bit [5]	Overflow of Port 5 Receive Packet Count
Bit [6]	Overflow of Port 6 Receive Packet Count
Bit [7]	Overflow of Port 7 Receive Packet Count
Bit [8]	Overflow of Port 8 Receive Packet Count
Bit [9]	Overflow of Port 0 Receive Packet Byte Count
Bit [10]	Overflow of Port 1 Receive Packet Byte Count
Bit [11]	Overflow of Port 2 Receive Packet Byte Count

Bit [12]	Overflow of Port 3 Receive Packet Byte Count
Bit [13]	Overflow of Port 4 Receive Packet Byte Count
Bit [14]	Overflow of Port 5 Receive Packet Byte Count
Bit [15]	Overflow of Port 6 Receive Packet Byte Count
Bit [16]	Overflow of Port 7 Receive Packet Byte Count
Bit [17]	Overflow of Port 8 Receive Packet Byte Count

Over Flow Flag 0: Register 0x3bh

Configuration	Description
Bit [0]	Overflow of Port 0 Transmit Packet Count
Bit [1]	Overflow of Port 1 Transmit Packet Count
Bit [2]	Overflow of Port 2 Transmit Packet Count
Bit [3]	Overflow of Port 3 Transmit Packet Count
Bit [4]	Overflow of Port 4 Transmit Packet Count
Bit [5]	Overflow of Port 5 Transmit Packet Count
Bit [6]	Overflow of Port 6 Transmit Packet Count
Bit [7]	Overflow of Port 7 Transmit Packet Count
Bit [8]	Overflow of Port 8 Transmit Packet Count
Bit [9]	Overflow of Port 0 Transmit Packet Byte Count
Bit [10]	Overflow of Port 1 Transmit Packet Byte Count
Bit [11]	Overflow of Port 2 Transmit Packet Byte Count
Bit [12]	Overflow of Port 3 Transmit Packet Byte Count
Bit [13]	Overflow of Port 4 Transmit Packet Byte Count
Bit [14]	Overflow of Port 5 Transmit Packet Byte Count
Bit [15]	Overflow of Port 6 Transmit Packet Byte Count
Bit [16]	Overflow of Port 7 Transmit Packet Byte Count
Bit [17]	Overflow of Port 8 Transmit Packet Byte Count

Over Flow Flag 2: Register 0x3ch

Configuration	Description
Bit [0]	Overflow of Port 0 Collision Count
Bit [1]	Overflow of Port 1 Collision Count
Bit [2]	Overflow of Port 2 Collision Count

Bit [3]	Overflow of Port 3 Collision Count
Bit [4]	Overflow of Port 4 Collision Count
Bit [5]	Overflow of Port 5 Collision Count
Bit [6]	Overflow of Port 6 Collision Count
Bit [7]	Overflow of Port 7 Collision Count
Bit [8]	Overflow of Port 8 Collision Count
Bit [9]	Overflow of Port 0 Error Count
Bit [10]	Overflow of Port 1 Error Count
Bit [11]	Overflow of Port 2 Error Count
Bit [12]	Overflow of Port 3 Error Count
Bit [13]	Overflow of Port 4 Error Count
Bit [14]	Overflow of Port 5 Error Count
Bit [15]	Overflow of Port 6 Error Count
Bit [16]	Overflow of Port 7 Error Count
Bit [17]	Overflow of Port 8 Error Count

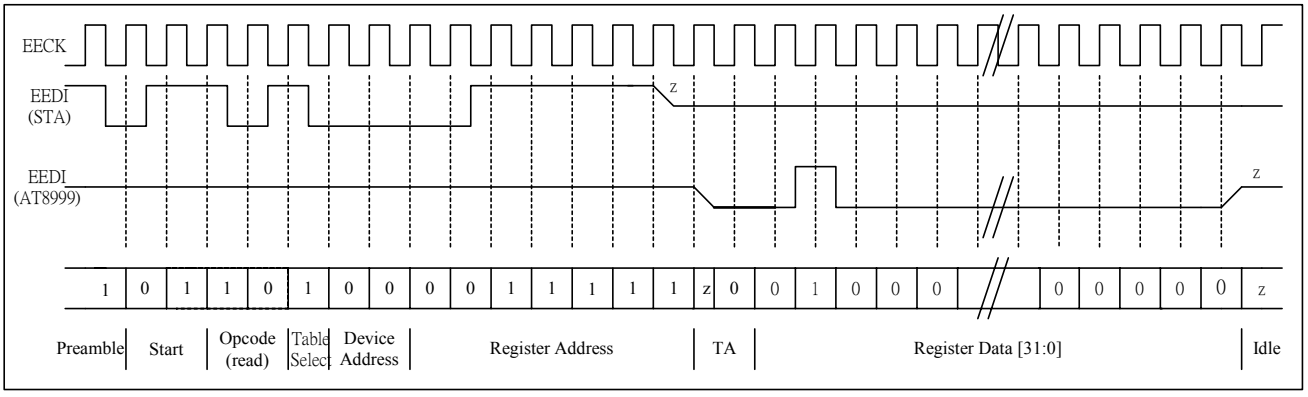
4.3 Serial Interface Timing

ADM6999G serial chip internal counter or EEPROM access timing.

EESK: Similar as MDC signal.

EDI: Similar as MDIO.

ECS: Must keep low.



Preamble: At least 32 continuous “1”.

Start: 01(2 bits)

Opcode: 10 (2 bits, Only supports read command)

Table select: 1/Counter, 0/ EEPROM (1 bit)

Register Address: Read Target register address. (7 bits)

TA: Turn Around.

Register Data: 32 bit data.

Counter output bit sequence is bit 31 to bit 0.

If user read EEPROM then 32 bits data will separate as two EEPROM registers. The sequence is:

Register +1, Register (Register is even number).

Register, Register-1(Register is Odd number).

Example: Read Register 00h then ADM6999G will drive 0x01h & 0x00h.

Read Register 03h then ADM6999G will drive 0x03h & 0x02h.

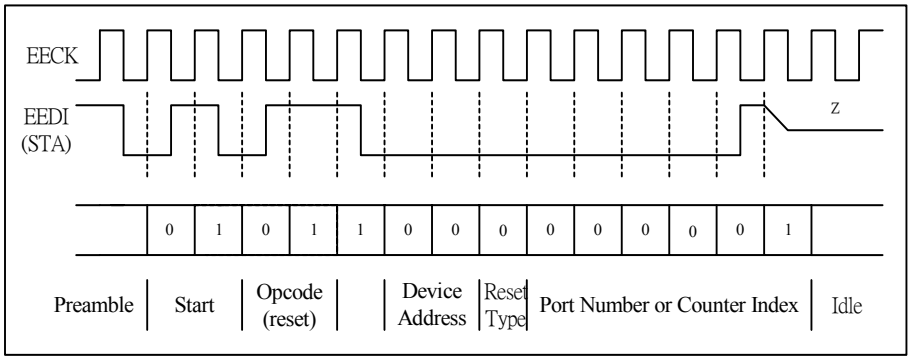
Idle: EESK must send at least one clock at idle time.

ADM6999G issue Reset internal counter command

EESK: Similar as MDC signal.

EDI: Similar as MDIO.

ECS: Must keep low.



Preamble: At least 32 continuous “1”.

Start: 01(2 bits)

Opcode: 01 (2 bits, Reset command)

Device Address: Chip physical address as PHYAS[1:0].

Reset_type: Reset counter by port number or by counter index.

1: Clear dedicate port’s all counters.

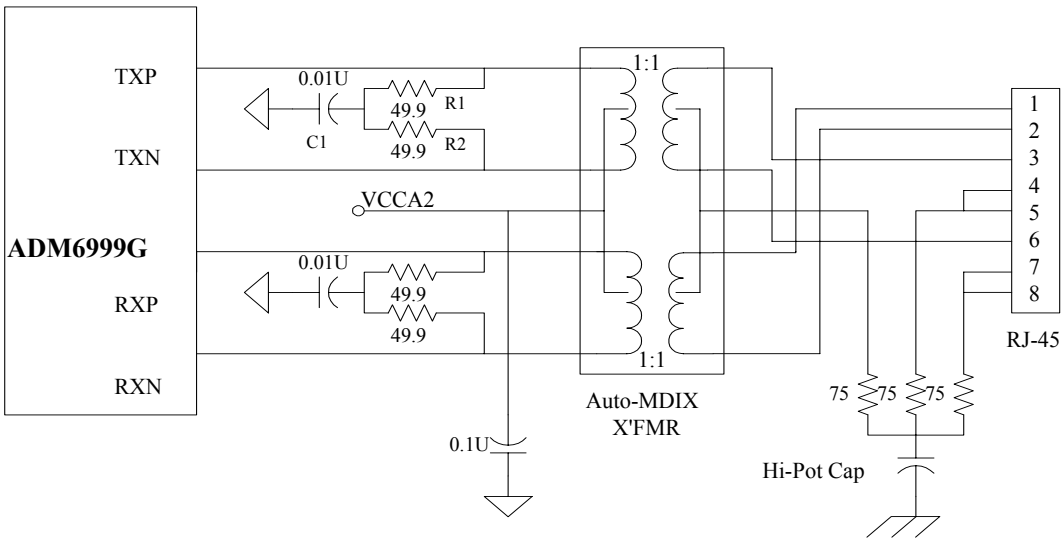
0: Clear dedicate counter.

Port_number or counter index: User define clear port or counter.

Idle: EECK must send at least one clock at idle time.

5. TX/FX Interface

5.1 TP Interface



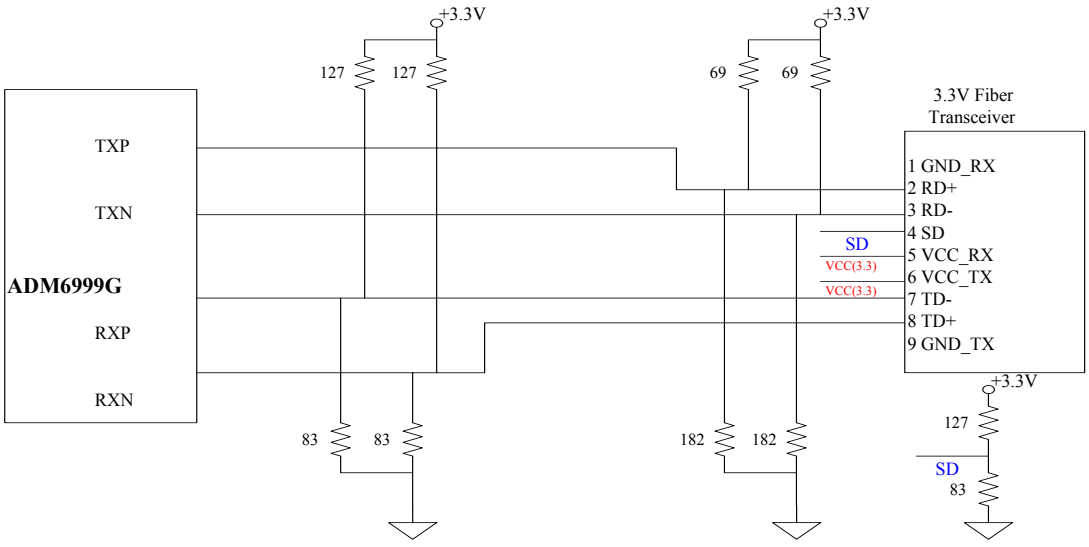
Transformer requirement:

. TX/RX rate 1:1

. TX/RX central tap connect together to VCCA2.

User can change TX/RX pin for easy layout but do not change polarity. ADM6999G supports auto polarity on receiving side.

5.2 FX Interface



6. DC Characteristics

6.1 Absolute Maximum Rating

Symbol	Parameter	Rating	Units
V_{CC}	Power Supply	-0.3 to 3.63	V
Vcca2	TX line driver	1.8	V
Vccpll	PLL voltage	1.8	V
Vccik	Digital core voltage	1.8	V
V_{IN}	Input Voltage	-0.3 to V_{CC} + 0.3	V
Vout	Output Voltage	-0.3 to Vcc + 0.3	V
T_{STG}	Storage Temperature	-55 to 155	°C
PD	Power Dissipation	1.8	W
ESD	ESD Rating	2KV	V

6.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	2.8	3.3	3.465	V
Vcca2	TX line driver	1.7	1.8	1.9	V
Vccpll	PLL voltage	1.7	1.8	1.9	V
Vccik	Digital core voltage	1.7	1.8	1.9	V
Vin	Input Voltage	0	-	Vcc	V
PC	Power consumption		1.8		W
Tj	Junction Operating Temperature	0	25	115	°C

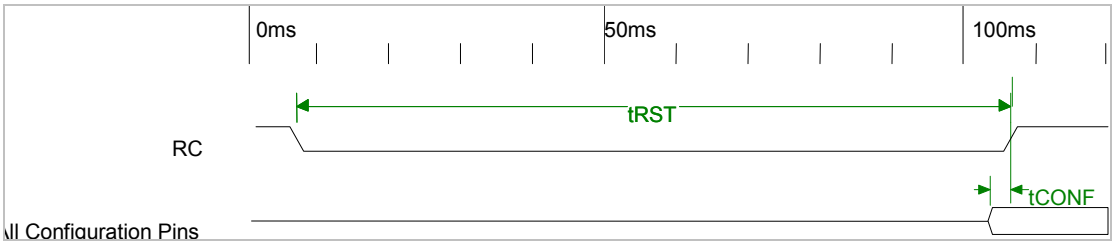
6.3 DC Electrical Characteristics for 3.3V Operation

Under Vcc=3.0V~3.6V, Tj= 0 °C ~ 115 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	CMOS			0.3 * Vcc	V
V_{IH}	Input High Voltage	CMOS	0.7 * Vcc			V
V_{OL}	Output Low Voltage	CMOS			0.4	V
V_{OH}	Output High Voltage	CMOS	0.7 * Vcc			V
R_I	Input Pull_up/down Resistance	V_{IL}=0V or V_{IH} = Vcc		100		KΩ

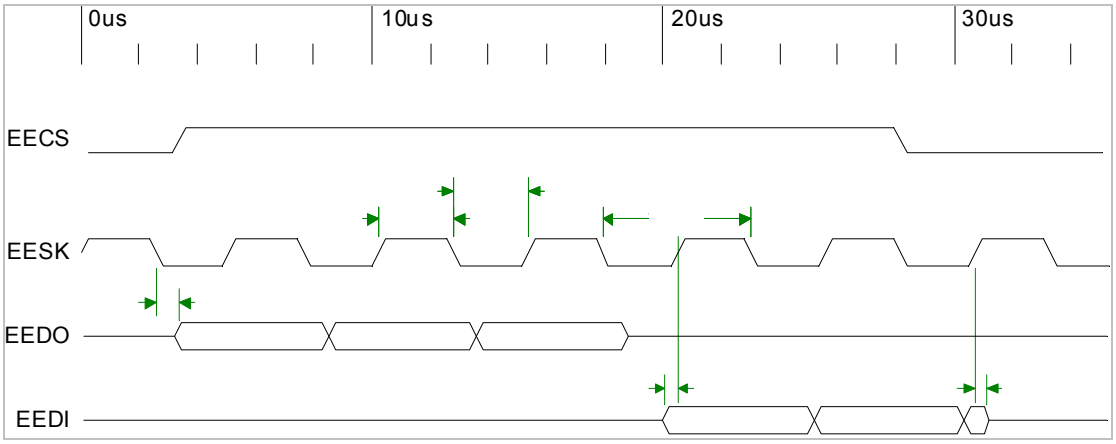
7. AC Characteristics

7.1 Power On Reset



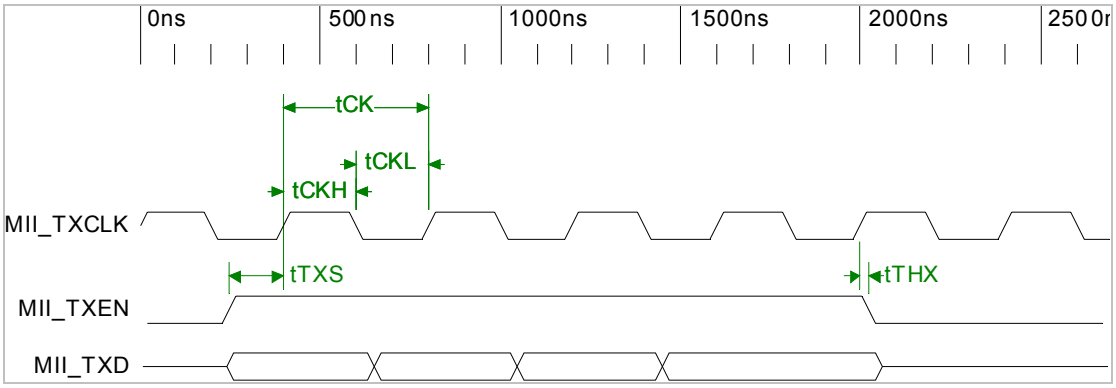
Symbol	Parameter	Conditions	Min	Typ	Max	Units
TRST	RST Low Period		100			ms
TCONF	Start of Idle Pulse Width		100			ns

7.2 EEPROM Data Timing



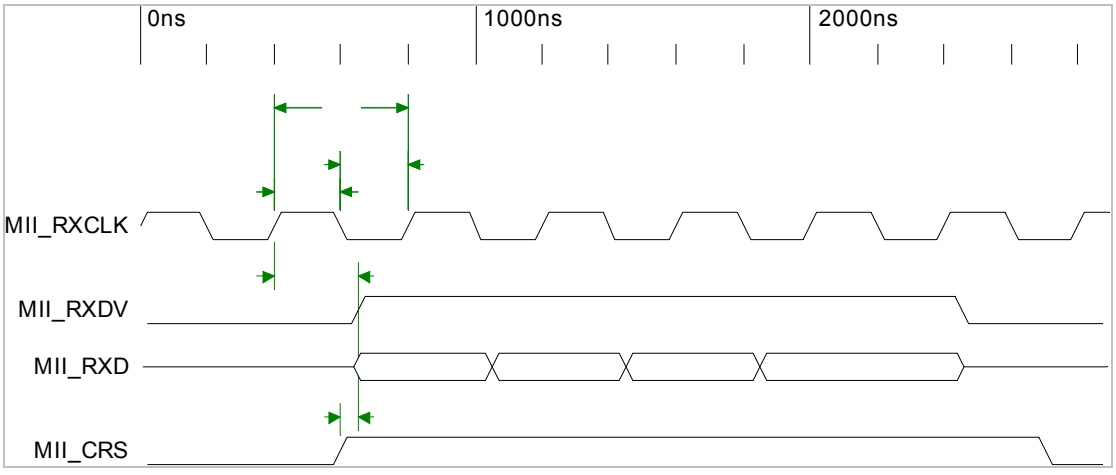
Symbol	Parameter	Conditions	Min	Typ	Max	Units
TESK	EESK Period			5120		ns
TESKL	EESK Low Period		2550		2570	ns
TESKH	EESK High Period		2550		2570	ns
TERDS	EEDI to EESK Rising Setup Time		10			ns
TERDH	EEDI to EESK Rising Hold Time		10			ns
TEWDD	EESK Falling to EEDO Output Delay Time				20	ns

7.3 10Base-TX MII Input Timing



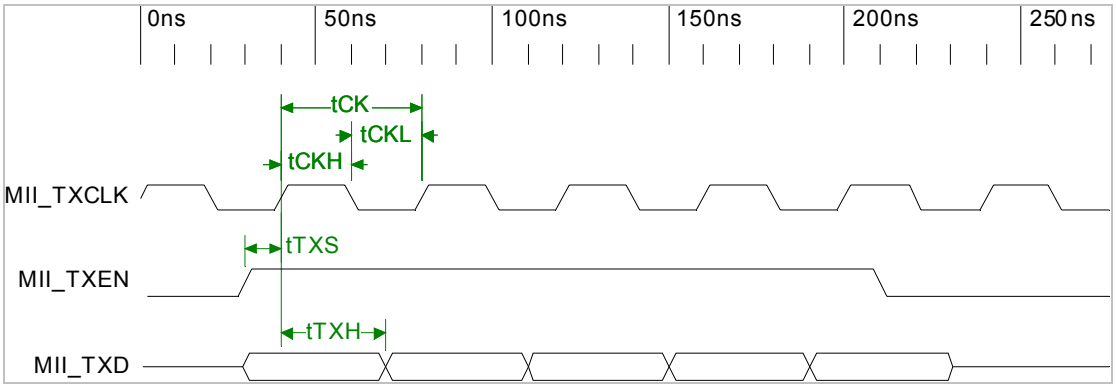
Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCK	MII_TXCLK Period			400		ns
TCKL	MII_TXCLK Low Period		160		240	ns
TCKH	MII_TXCLK High Period		160		240	ns
TTXS	MII_TXD, MII_TXEN to MII_TXCLK Rising Setup Time		10			ns
TTXH	MII_TXD, MII_TXEN to MII_TXCLK Rising Hold Time		10			ns

7.4 10Base-TX MII Output Timing



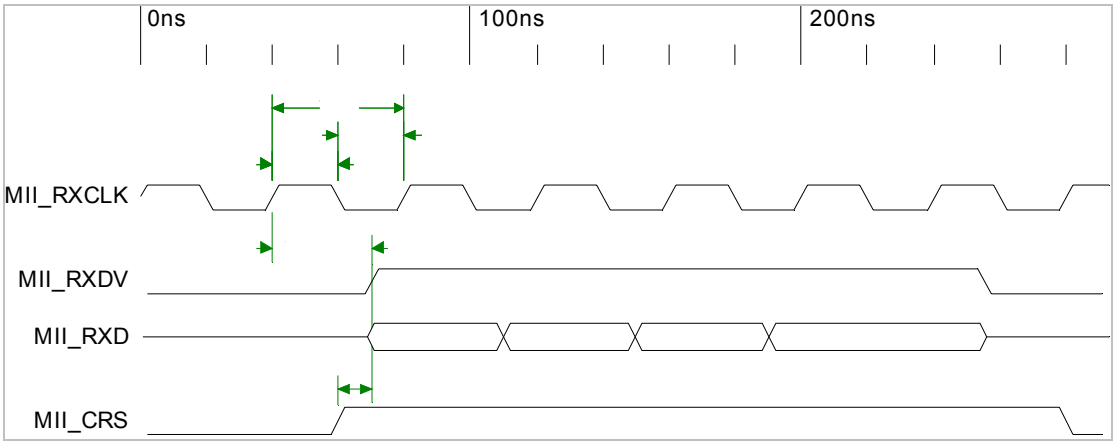
Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCK	MII_RXCLK Period			400		ns
TCKL	MII_RXCLK Low Period		160		240	ns
TCKH	MII_RXCLK High Period		160		240	ns
TCSVA	MII_CRS Rising to MII_RXDV Rising		0		10	ns
TRXOD	MII_RXCLK Rising to MII_RXD, MII_RXDV, MII_CRS Output Delay		200			ns

7.5 100Base-TX MII Input Timing



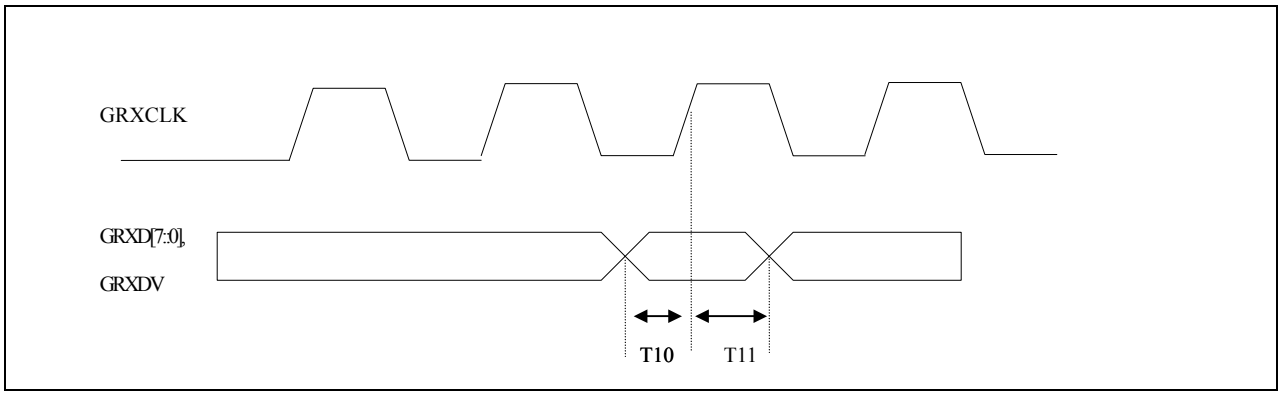
Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCK	MII_TXCLK Period			40		ns
TCKL	MII_TXCLK Low Period		16		24	ns
TCKH	MII_TXCLK High Period		16		24	ns
TTXS	MII_TXD, MII_TXEN to MII_TXCLK Rising Setup Time		10			ns
TTXH	MII_TXD, MII_TXEN to MII_TXCLK Rising Hold Time		10			ns

7.6 100Base-TX MII Output Timing



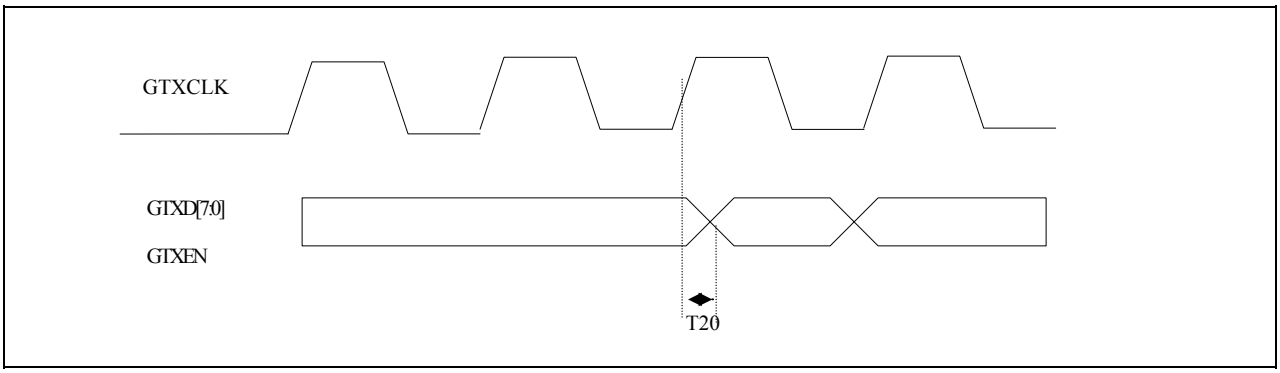
Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCK	MII_RXCLK Period			40		ns
TCKL	MII_RXCLK Low Period		16		24	ns
TCKH	MII_RXCLK High Period		16		24	ns
TCSVA	MII_CRS Rising to MII_RXDV Rising		0		10	ns
TRXOD	MII_RXCLK Rising to MII_RXD, MII_RXDV, MII_CRS Output Delay		20		30	ns
TEWDD	EESK Falling to EEDO Output Delay Time				20	ns

7.7 GMII Receive Signals Timing



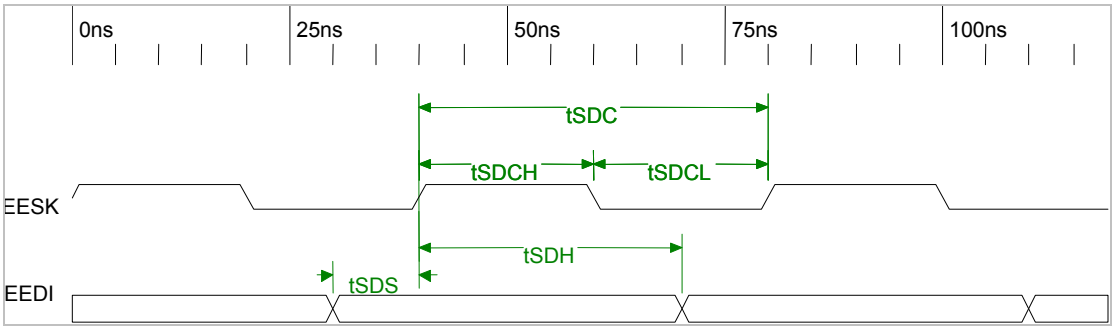
Name	Parameter	Min	Max	Units
T10	Setup Time to Rising GRXCLK	2		ns
T11	Hold Time to Rising GRXCLK	0.5		ns

7.8 GMII Transmit Signals Timing



Name	Parameter	Min	Max	Units
T20	Data Valid Delay after Rising GTXCLK	1.5	4	ns

7.9 SMI Timing



Symbol	Parameter	Conditions	Min	Typ	Max	Units
TCK	EESK Period		20			ns
TCKL	EESK Low Period		10			ns
TCKH	EESK High Period		10			ns
TSDS	EEDI to EESK rising setup time on read/write cycle		4			ns
TSDH	EEDI to EESK rising hold time on read/write cycle		2			ns

8. Package

128 Pin PQFP Outside Dimension